APPLICATION NOTE

Application and Product Description of the 16:9 Compressor SAA4981/T

AN96018

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Abstract

The SAA 4981/T is a monolithic integrated 16:9 Compressor for TV applications. It is providing a fixed horizontal compression for luminance and colour difference signals to adapt the geometry by displaying a 4:3 coded video signal on a 16:9 picture screen.

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Summary

This report describes the principle function of the 16:9 Compressor SAA 4981 and is intended to provide application support for designing in of the circuit.

The SAA 4981 is an analog one-chip and alignment free IC, designed in a standard CMOS process. The chip provides horizontal compressing of base-band video signals to adapt the geometry for displaying 4:3 coded video signals on a 16:9 picture screen. The device is delivered as SAA4981 with a 24pin DIL package and as SAA4981T with a 24pin SMD package.

Three signal paths for the luminance and the colour difference signals are available, all with an input bandwidth up to 5 MHz. The compressed video signals can be shifted to three different screen positions or two bypass modes can be used. The modes are controlled via three control pins. All pre- and post-filters together with the clock- and control processing are integrated.

After the introduction, given in the first chapter, the second chapter describes the principal function of the 16:9 Compressor. Chapter 3 shows the realization of the 16:9 Compressor function and gives a description of the signal and control processing inside the SAA 4981.

The pinning and more detailed information about the pin application are given in chapter 4.

Two system applications using the 16:9 Compressor are given in chapter 5, followed by two application examples of the SAA 4981 and one example for the SAA4981T in chapter 6.

A conclusion is given in chapter 7.

This application note is based on the report AN94028 [1], where the application hints are given for only the DIL version of the SAA4981.

CONTENTS

1. Introduction

Following today's trend of introducing high definition TV a new screen format for video productions was proposed by the broadcasters and TV set makers: the 16:9 format. Consequently the picture tubes of a TV set must be adapted to this format.

Because of the compatibility of the conventional 4:3 and the new 16:9 format both systems are using for PAL standards a line frequency of 15625 Hz with an active video part of 52 µs. In the future it must be also possible to broadcast "old" 4:3 format TV productions. If now such a conventional coded video signal is displayed on a new 16:9 picture tube geometry errors will occur. The video pictures are displayed too wide, as it is shown in figure 1.

To correct the geometry the video information must be adapted to the 16:9 screen. This can be done in the vertical or horizontal direction.

A vertical expansion causes the disadvantage to lose informations at the beginning and the end of a vertical period. Changing the horizontal deflection the screen will be underscanned. Also all effects of the horizontal deflection like ringing will be visible within the picture.

Another possibility is to compress the video signals in horizontal direction. This can be done inside the video signal processing part without changing the deflection as shown in figure 2. Such a compression can be realized using the 16:9 Compressor SAA 4981.

This note is based on [1]. After the SAA4981T is available it is necessary to give also application hints for this device.

2. Principal Function of a 16:9 Compressor

To adapt the geometry of a 4:3 coded video signal for displaying it on a 16:9 picture tube without losing of information, this signals must be horizontal compressed by a factor 3:4.

This will be possible using a memory. A functional blockdiagram is shown in figure 3. Writing the video signal into the memory with a clock frequency f_{in} and reading out the signal one line period later with a clock frequency of $f_{out} = 4 * f_{in}/3$, a compression of the factor 3:4 is done. Parallel writing and reading in each signal path can be realized using two line memories. The write/read cycle alternates from line to line. This results in an output video signal with a correct geometry during the active video part, shown in figure 2.

By linear compressing of the video signals with a factor of 3:4, all included signal frequencies are transferred to a higher frequency band. This is done with the inverse compression factor of 4:3, seen in figure 4. To avoid errors for the modulated chrominance inside a CVBS signal or for sync signals, the compression is best done after the colour decoding in the base-band domain. The luminance Y and both colour difference signals (R-Y) and (B-Y) are compressed in this way.

After compression of the active video part as shown in figures 2 and 4, side panels remain on the screen. The side panels can be filled internally with the black level clamping signal of the video signal.

To provide an one-chip solution the clock and control processing have to be integrated.

3. Internal Signal Processing of the 16:9 Compressor SAA 4981

The 16:9 Compressor SAA 4981 is an analog one-chip and alignment free IC, designed in a standard CMOS process. The chip provides horizontal compressing of base-band video signals to adapt the geometry for displaying 4:3 coded video signals on a 16:9 picture tube.

Figure 5 shows the SAA 4981 in block form. The main parts of the IC - the line memories, the control and clock processing - are described in the following chapters.

3.1 Line Memories

Line Memories are used for the compression. Using a standard CMOS process allows the design of line memories in the switched-capacitor technique and an implementation inside the analog environment of an analog video signal processing chip.

Figure 6 shows the principal function of a switched-capacitor memory cell. If switch S_{in} is closed, storage capacitor C_S is charged to the momentary amplitude of the input signal available on the input write-rail. With the trailing edge of the S_{in} control pulse the capacitor C_S and the input rail are disconnected and the voltage is stored. After time T, the charge is applied to the output read-rail by closing switch S_{out}. The stored voltage is read out by a sense amplifier. A memory cell can be read-out only once.

Figure 7 shows the principle architecture of a switched-capacitor line memory by using multiple memory cells parallel and controlling the write/read switches with a shift register. Shifting a single pulse through the shift register the storage capacitors are charged in sequence with the momentary input voltage of the input write-rail by closing the switches S_{in}. The same shift register also controls the switches S_{out}. The control of the read- and write-switches is made in a way that a capacitor is first read-out and after that loaded with a new value.

The storage time of one cell is defined by the time between a write and a read pulse. The step time from one storage capacitor to the next one - or sampling rate - depends on the clock frequency. The switched-capacitor technique is a time discrete but amplitude continuous method of signal processing. Amplitude quantization errors, which are common in digital signal processing, are not generated. A simple, integrated, reconstruction low-pass filter converts the signals from the time discrete domain back to the time continuous domain.

To avoid problems between writing and reading the memory, the 16:9 Compressor uses for each signal path two line memories LM1 and LM2. This is shown in figure 8.

The compression is done in the following way: Writing the input signal into line memory LM1 using the clock f_{in} and at the same time reading LM2 with f_{out}. One line period later LM1 is in the read mode using f_{out} and LM2 is in the write mode using f_{in}. In front of the shift register a multiplexer selects the required clock. The compression ratio is defined as the relation between both clocks:

f_{in} = 13.5 MHz
f_{out} = 18.0 MHz
f_{in} / f_{out} = 3/4.

In case of no compression the clocks for writing and reading are identical:

$f_{in} = f_{out}$ = 13.5 MHz
f_{in} / f_{out} = 1.

The delay between the input signal and output signal is one line period. No horizontal processing delay is done.

The output multiplexer MUX SC-LINE MEMORIES selects the line memory which is momentary in the read mode.

The clocks and the control signals are generated in the 54 MHz PLL and the CONTROLLER, which are described in chapter 3.4 and 3.5.

3.2 Video Signal In- / Outputs

Three video inputs are available. One for the luminance Y≡Y_IN and two for the colour difference signals (B Y) ≡ (B-Y)_IN and (R-Y) ≡ (R-Y)_IN. Both polarities for the colour difference signals are possible: ± (R-Y), ± (B-Y). The input levels are specified according to the CCIR recommendation 471-1. The typical input voltage for the luminance is 320 mV with a tolerance of ± 3 dB. The (B-Y) input voltage is 1.33 V and 1.05 V for (R-Y), both also with a tolerance of ± 3 dB. The input signals are ac coupled and internal clamped.

Three on-chip low-pass filters LPF_5.0 with a bandwidth up to 5.0 MHz are used as anti-aliasing pre-filters for the time discrete signal processing and also to provide EMC (electromagnetic compatibility) distortions. Because of using three identical pre-filters it is possible to process colour difference signals with a bandwidth up to 5.0 MHz.

The typical gain video input to output of the SAA4981 is 0dB.

The on-chip low-pass post-filters LPF_6.7 transfer the video signals from the discrete time domain back to the continuous time domain. The increased cutoff frequency of 6.7 MHz is adapted to the implemented compression factor: Because of reading the line memories with a higher frequency compared to the writing frequency, the video frequencies are transferred to a higher frequency band, like it is shown in figure 4. This is done with the inverse compression ratio of 4:3. A 5.0 MHz input frequency is transferred in the compression mode up to 6.67 MHz.

The frequency response for all three signal paths is specified for input frequencies up to 5.0 MHz. No restrictions for the colour difference signals will be done.

3.3 Compression Modes and Side Panels

Different modes for compression and by-pass are available.

For the by-pass function two modes can be used:
First a full by-pass mode, without using the line memories. The input signals are directly fed via the input clamping to the outputs. No filtering and signal processing is done.
The second by-pass mode uses the line memories with $f_{in} = f_{out} = 13.5$ MHz for writing and reading. The output signals have the described delay of one line period.

In the compression modes additional side panels are generated, as shown in figure 9.It is possible to place the compressed active video part at different positions on the screen: left -, centre - and right position.
The remaining side panels can be filled with external signals via the inputs Y_SIDE, BY_SIDE and RY_SIDE (figure 4). Y_SIDE provides the luminance signal path Y_chanel. For the colour difference signal paths BY_SIDE provides the (B-Y)_channel and RY_SIDE the (R_Y)_channel. These signals can be referred to the black level reference signal of the IC, which is available at pin CLA_OUT. Connecting Y_SIDE, BY_SIDE and RY_SIDE directly to CLA_OUT black side panels are generated.

Switching between the compressed active video and the side panels is done in the output multiplexer MUX_Y, MUX_BY and MUX_RY. The control signals C1, C2 and C3 are generated inside the controller. Also the switching between the compression modes and both by-pass modes is done in the output multiplexer.

3.4 Control and Clock Processing

The control and clock processing (block controller in figure 4) generates the clocks for the time discrete signal processing and all timing control signals for the IC.

For the clock generation a line locked 54 MHz PLL is provided which is synchronized with the external HREF signal. HREF is a line frequent burst key signal. The high level input voltage for the HREF signal is specified between 3.0 V and 6.5 V. The slicing level for the HREF signal is automatically adapted to the input voltage: 0.5 V ... 1.0 V below top. Adapting a sandcastle signal to this specification the included burst key pulse is used. The timing is described in chapter 3.6. The H-Separation detects the incoming analog signal and converts it to a digital H_REF signal for the synchronization of the 54 MHz PLL and for generating the control signals. Inside the PLL the 54.0 MHz clock is divided down to 13.5 MHz and 18.0 MHz. Both clocks are used for the line memories and the controller.

The generation of the timing control signals are based on the 18.0 MHz clock and referred to the H_REF signal.

3.5 Mode Control

With three external control signals CTRL1, CTRL2 and CTRL3 the controller selects the different modes (two by-pass and three compression modes):

CTRL1	CTRL2	CTRL3	Mode
LOW	LOW	LOW	by-pass mode via the line memories
LOW	LOW	HIGH	full by-pass mode not through the line memories
LOW	HIGH	LOW	compression mode, left position
HIGH	LOW	LOW	compression mode, centre position
HIGH	HIGH	LOW	compression mode, right position

The pin TEST is only used for internal testing the IC and has to be connected to digital ground for normal operation mode.

3.6 Timing and Video Standards

The timing of the by-pass and compression modes, described in figure 10, refers to the incoming video and HREF signals.

In the full by-pass mode the complete input video signals are fed directly to the output stages. In the by-pass mode via the line memories only the 52 µs part of the active video signals, sampled into the line memories, are available at the outputs. The blanking period of the video signals of 12 µs are set to a black level signal. The sampling window for the video signals is defined by the HREF signal based timing.

In the compression modes only a 49 µs window of the active video is used. A reserve for the overwriting on the picture tube of maximal 1.5 µs for the left and right side (52 µs - 2 ∗ 1.5 µs = 49 µs) is preserved.

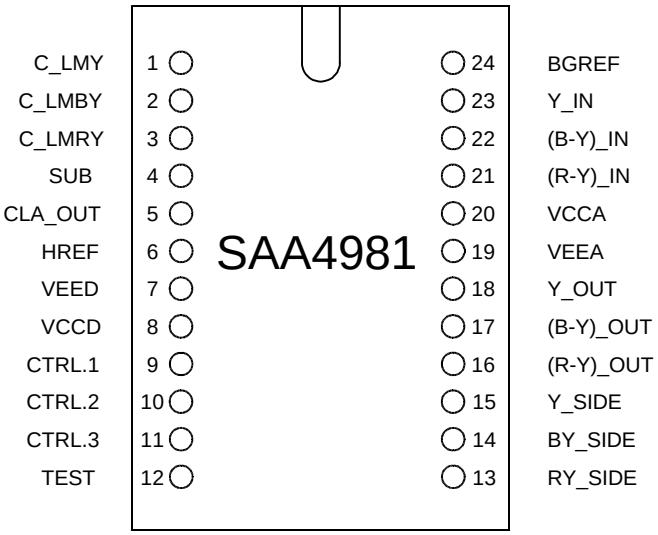
The following video standards can be processed with the 16:9 Compressor: B / C / G / H / M / N.

It is also possible to process the standards D / I / K / K1 / L with the result of a reduced bandwidth above 5.0 MHz (referred to the input signal).

3.7 Clamping

The video signals are clamped at the input and inside the processing chain of the IC to generate correct DC levels for the signal processing and the internal switches (input clamping, line memories and multiplexer). The clamp signals are generated in the controller section and the clamping reference signals in the block CLAMP REFERENCE. For storing the clamping reference voltages external capacitors are necessary, connected as close as possible to the input pins C_LMY, C_LMBY, C_LMRY and BGREF.

4. Pinning and packages of the SAA4981



Package for SAA4981:DIL24

Package for SAA4981T:SO24

TABLE 1 Pinning SAA4981

4.1 Pin names and short description

SYMBOL	PIN	DESCRIPTION
C_LMY	1	decoupling capacitor for Y reference voltage
C_LMBY	2	decoupling capacitor for U reference voltage
C_LMRY	3	decoupling capacitor for V reference voltage
SUB	4	substrate connection (see application information)
CLA_OUT	5	internal clamping reference voltage output
HREF	6	horizontal reference input
VEED	7	ground for digital section
VCCD	8	positive digital supply voltage
CTRL.1	9	control input 1
CTRL.2	10	control input 2
CTRL.3	11	control input 3
TEST	12	test signal
RY_SIDE	13	side panel input signal for V
BY_SIDE	14	side panel input signal for U
Y_SIDE	15	side panel input signal for Y
(R-Y)_OUT	16	output signal for (R-Y)

SYMBOL	PIN	DESCRIPTION
(B-Y)_OUT	17	output signal for (B-Y)
Y_OUT	18	output signal for Y
VEEA	19	ground for analog section
VCCA	20	positive analog supply voltage
(R-Y)_IN	21	input signal for (R-Y)
(B-Y)_IN	22	input signal for (B-Y)
Y_IN	23	input signal for Y
BGREF	24	decoupling capacitor for internal reference voltage

TABLE 2 SAA4981 Pin names and short description

4.2 Pin applications

Detailed information about the characteristics of the pins is given in the data sheet[2].

Pin1: C_LMY

Pin for the external decoupling capacitor for the internal Y reference voltage.

Recommended value is 100nF

Pin2: C_LMBY

Pin for the external decoupling capacitor for the internal U reference voltage.

Recommended value is 100nF

Pin3: C_LMRY

Pin for the external decoupling capacitor for the internal V reference voltage.

Recommended value is 100nF

Pin4: SUB

The substrate has to be connected to VEED

Pin5: CLA_OUT

Output of the internal clamping voltage.

This voltage could be used to generate the side panel voltages. The max. allowed load is 160uA/30pF.

Pin6: HREF

Input for the horizontal reference signal.

The raising edge is used as reference. For detailed information of the behaviour of the slicing level see chapter ‘Control and Clock Processing.
To protect the PLL-system against double-trigger the raising and the trailing edge of the reference signal should be not disturbed.

Pin7: VEED

Ground for the digital part.

For best picture performance the influence between the VEED-current and the VEEA-current has to be lowered as much as possible by the PCB layout (see also chapter ‘Application of the 16:9 compressor‘).

Pin8: VCCD

Positive supply voltage for digital part.

An external low-pass filter for the VCC rail has to be placed as near as possible to this pin to reduce the influence of the VCCD supply current to other parts of the circuit (e.g. VEEA rail).
Values for the capacitors and the resistor depend on the PCB layout (see also chapter ‘Application of the 16:9 compressor‘).

Pin9: CTRL.1

Input for control signal 1.

The compress mode is controlled via this pins 9 (CTRL.1), 10 (CTRL.2) and 11 (CTRL.3)).

CTrl.1 (pin 9)	CTrl.2 (pin 10)	CTrl.3 (pin 11)	Function
L	L	L	Bypass through delay lines
L	H	L	Compression left position
H	L	L	Compression centre position
H	H	L	Compression right position
L	L	H	Bypass not through delay lines

Pin10: CTrl.2

Input for control signal 2.

The compress mode is controlled via this pins 9 (CTRL.1), 10 (CTRL.2) and 11 (CTRL.3). Detailed information see pin 9.

Pin11: CTrl.3

Input for control signal 3.

The compress mode is controlled via this pins 9 (CTRL.1), 10 (CTRL.2) and 11 (CTRL.3)). Detailed information see pin 9.

Pin12: TEST

For normal operation not used.

Has to be connected to ground (VEED).

Pin13: RY_SIDE

Input for the DC-coupled RY-side signal for the (R-Y)-channel.

Additional information see chapter ‘Compression Modes and Side Panels‘.

Pin14: BY_SIDE

Input for the DC-coupled BY-side signal for the (B-Y)-channel.

Additional information see chapter ‘Compression Modes and Side Panels‘.

Pin15: Y_SIDE

Input for the DC-coupled Y-side signal for the Y-channel.

Additional information see chapter ‘Compression Modes and Side Panels‘.

Pin16: (R-Y)_OUT

Output pin for the processed (R-Y) signal.

Typical gain pin 21 to pin 16 is 0dB.

Pin17: (B-Y)_OUT

Output pin for the processed (B-Y) signal.

Typical gain pin 22 to pin 17 is 0dB.

Pin18: Y_OUT

Output pin for the processed Y signal.

Typical gain pin 23 to pin 18 is 0dB.

Pin19: VEEA

Ground for the analog part.

For best picture performance the influence between the VEED-current and the VEEA-current has to be lowered as much as possible by the PCB layout (see also chapter ‘Application of the 16:9 compressor‘).

Pin20: VCCA

Positive supply voltage for analog part.

A low-pass filter with a decoupling capacitor from pin 20 to pin 19 and a resistor to the VCC rail has to be placed as near as possible to the device.
Values for the capacitor and resistor depend on the PCB layout (see also chapter ‘Application of the 16:9 compressor‘).

Pin21: (R-Y)_IN

Input for the AC coupled (R-Y) signal.

Recommended value for the capacitor is 2.2nF.

Pin22: (B-Y)_IN

Input for the AC coupled (B-Y) signal.

Recommended value for the capacitor is 2.2nF.

Pin23: Y_IN

Input for the AC coupled Y Signal.

Recommended value for the capacitor is 2.2nF.

Pin24: BGREF

Decoupling capacitor for internal reference voltage.

Recommended value is 100nF.

5. System Applications

The SAA 4981 is designed for applications in the base-band signal interface.

Figure 11 shows a system application diagram as an example at which location the 16:9 Compressor SAA 4981 can be inserted. A colour decoder TDA 9162 together with the base-band delay line TDA 4661 is used to decode the CVBS or YC input signals to the luminance Y’ and the base-band colour difference signals -(B-Y)’ and -(R-Y)’. Filters for luminance and chrominance separation are integrated inside the decoder. The decoder provides also all signals which are necessary for the video processor and the output deflection stages including a sandcastle signal used in the 16:9 Compressor. The TDA 9162 offers also the possibility to adapt the picture size on a 16:9 picture tube in the vertical direction by vertical compression and expansion.

To control the SAA 4981 an I^2C bus interface PCF 8574 for generating the control signals CRTL1, CRTL2 and CRTL3 can be used.

The outputs of the 16:9 Compressor are directly coupled by capacitors to the video processor family TDA 468∗ inputs, for example TDA 4687.

A system extension can be made with the circuit TDA 4670/71 (PSI). This circuit performs colour transient improvement and luminance peaking. A 16:9 Compressor SAA 4981 behind the PSI does not affect the improved bandwidth of the colour difference signals.

This as a further example for a system approach is shown in figure 12 with the colour decoder TDA 4655 and the sync-processor TDA 4690/91. The chrominance (CHR) and luminance (Y'') separation filters in front of the decoder are made in discrete technique.

The sync-processor TDA 4690/91 generates the sandcastle, horizontal HA and vertical VA impulses and a 13.5 MHz clock. The sandcastle signal is used as clamp and timing signal for the colour decoder, the base-band delay line and the 16:9 Compressor. The HA , the VA and the 13.5 MHz clock LLC signals are used for the deflection processor.

6. Application of the 16:9 Compressor

Two different general purpose applications with the SAA4981 are described. A third application uses the SAA4981T for a fully SMD layout.

The standard application, see figures 13.∗, shows the principal expenditure for using the 16:9 Compressor. The HREF input signal will be supplied by the decoder or sync processor and must be correlated to the input video signals as given in figure 10. This correlation is necessary to provide an exact centred compressed video output signal. Changing the above described correlation, for example additional delays in front of the SAA 4981, results in a visible shifted compressed video signal inside the sampling window on the screen.

A second application proposal, see figures 14.∗, allows the generation of a HREF signal referred to the incoming luminance signal. By this application all delays are compensated which results under all conditions in an exact centred compressed video signal. The generated HREF signal follows the delay of the previous signal processing, even this is switched as in case of TDA 4670/71 for colour transient improvement on/off.

The third application proposal, see figures 16.∗, is the 'SMD'-version of the second proposal and uses therefore the SAA4981T.

6.1 Standard Application of the 16:9 Compressor

The standard application is shown in figures 13.1 - 13.7.

Input signals for the application are the luminance YI, the colour difference signals -(B-Y)I, -(R-Y)I and an analog burst key signal HS, see figure 13-1. The video signals are coupled via capacitors to the 16:9 Compressor SAA 4981 as shown in figure 13-3. After the signal processing the non compressed/compressed signals are available at the outputs YO, -(B-Y)O and -(R-Y)O.

For the control of the by-pass and compression modes of the 16:9 Compressor an I^2C bus interface PCF 8574 is used (figure 13-4). The interface receives the I^2C bus signals SDA and SCL and generates the control signals CTRL1, CTRL2 and CTRL3. The salve address is 48_{hex} with subaddress 00_{hex}. The following coding is used:

00_{hex} : by-pass mode via the line memories
80_{hex} : full by-pass mode not through the line memories
40_{hex} : compression mode, left position
20_{hex} : compression mode, centre position
60_{hex} : compression mode, right position

Figure 13.3 shows a simple application for the side panel generation. The inputs Y_SIDE, BY_SIDE and RY_SIDE of the 16:9 Compressor are connected directly to pin CLA_OUT. Black side panels are generated, referred to the internal clamping level of the IC.

In the layout the wiring of the supply rails is important. The ground and the supply pins for the analog and digital sections of the IC are fed separately. A ground resistor R115 between GND and DGND (figure 13.2) is necessary to reduce disturbances which are produced inside the digital clock and control processing of the IC. Both supply voltages are filtered and stabilized for the circuit using two resistors R301, R302 and a capacitors C310 for +5VD and one resistor R300 and two capacitors C307, C308 for +5VA (+5VD ≡ digital supply voltage, +5VA ≡ analog supply voltage).

The 100 nF capacitors C300, C302, C304 and C301 (Pin 1 ≡ C_LMY, Pin 2 ≡ C_LMBY, Pin 3 ≡ C_LMRY, Pin 24 ≡ BGREF) are needed for the CLAMP REFERENCE block of the 16:9 Compressor.

All above described components, except R115, must connected as close as possible to the 16:9 Compressor IC package.

Figures 13.6 and 13.7 shows the layout of this application.

6.2 Application with a Delay Compensated HREF Input Signal

In the application, described in chapter 5 and 6.1, the HREF input signal referred e.g. to the CVBS signal at the input of the decoder or sync processor. In such a standard system application a PSI circuit TDA 4670/71 is often used, as it is shown in figure 12. This results in an additional delay. Also switching on/off of the CTI function results in different processing delays inside the TDA 4670/71. This will be visible by a non-exact centred compressed video output signal as described in chapter 6.

To eliminate the different delays between the HREF and the input signals of the SAA 4980/81, a new HREF signal must be derived directly from the luminance YI input signal of the 16:9 Compressor. This means that the YI signal must still carry the sync signal.

To generate the HREF signal a separate sync processor circuit like the TDA 4690/91 (SPC) can be used. This is shown in block form in figure 14.1. The application schematics and layout are shown in figures 14.2 - 14.9.

Figure 14.6 shows the application for the side panel generation. Blue side panels are used, which are referred to the black level reference signal of the 16:9 Compressor. This reference signal is available at pin CLA_OUT. All other parts directly used for the 16:9 Compressor are identical with the application described in chapter 6.1.

For the delay compensation the following application is added:

First an amplifier increases the reduced YI amplitude to the SPC input range (figure 14.2).

The SPC, shown in figure 14.3, can now generate a H-signal with four different positions (see figure 15). The positions can be controlled via pin 14. Because of the timing of the 16:9 Compressor (figure 10) the most centred picture position will be generated using the positive edge of the inverted H-signal. The H-signal is shifted to the left position (pin 14 of the SPC TDA 4690/91 connected to ground).

With this application the displayed picture is independent of all processing delays in front of the IC. Switching CTI on and off has now no influence to the visible picture content.

To adapt the SAA 4981 to other systems, for example NTSC M or using the separate SPC for other applications, it will be possible to use one of the other three H positions and/or the sandcastle pulse of the SPC.

6.3 SAA4981T-Application with a Delay Compensated HREF Input Signal

The implemented functions are the same as described in chapter 6.2, the DIL devices are changed to their corresponding SMD types. This is shown in block form in figure 16.1. The application schematics and layout are shown in figures 16.2 - 16.9.

For an optimized SMD-PCB it is necessary to change the low-pass filter in the digital supply rail to avoid influences between the digital and analog voltage rails. The changed circuit diagrams are shown in figure 16.2 for the supply part and figure 16.4 for the SAA4981T.

7. Conclusion

The SAA 4981 is a monolithic integrated 16:9 compressor which provides a fixed horizontal compression by a factor of 4:3 of the active video part. So it is possible to adapt the geometry by displaying a 4:3 coded video signal on a 16:9 picture screen. Three signal paths for the luminance and the colour difference signals are available, all with a bandwidth up to 5 MHz. The compressed video signals can be shifted to three different screen positions or bypass modes can be used. The modes can be controlled via three control pins. All pre- and post-filters together with the clock - and control processing are integrated, so that the IC is easy applicable.

8. References

[1] Application note AN94028
Title: 16:9 Compressor SAA4981
Author: F. Volmari

[2] Data sheet SAA4981/T (Oct.1995)

G. Onken

9. Figures

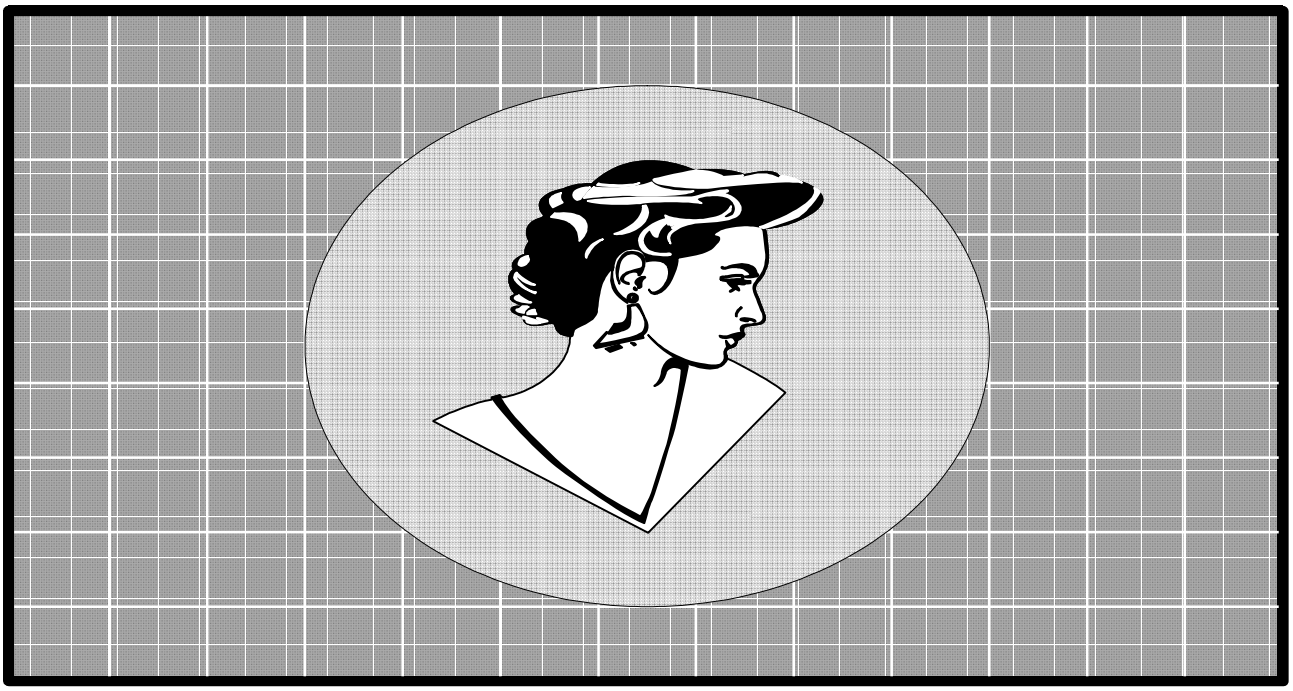


Fig. 1: 4 : 3 Coded Video Signal Displayed on a 16 : 9 Picture Tube

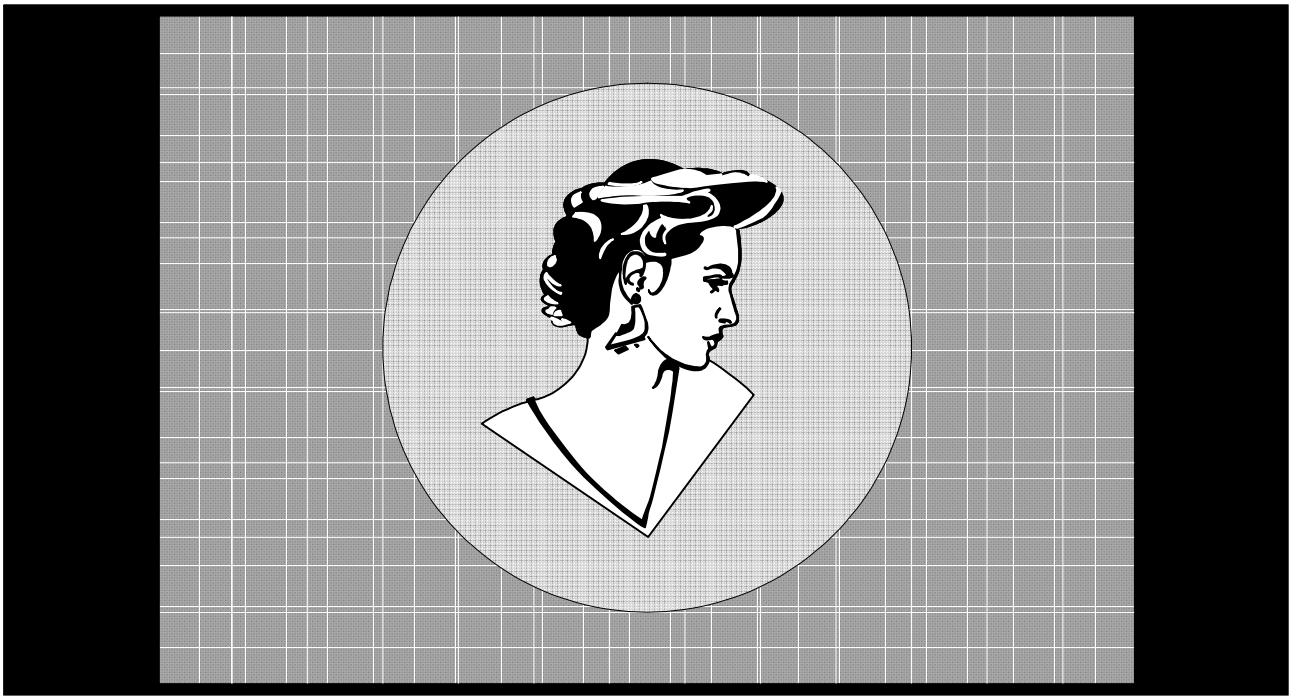


Fig. 2: Compressed 4 : 3 Coded Video Signal Displayed on a 16 : 9 Picture Tube

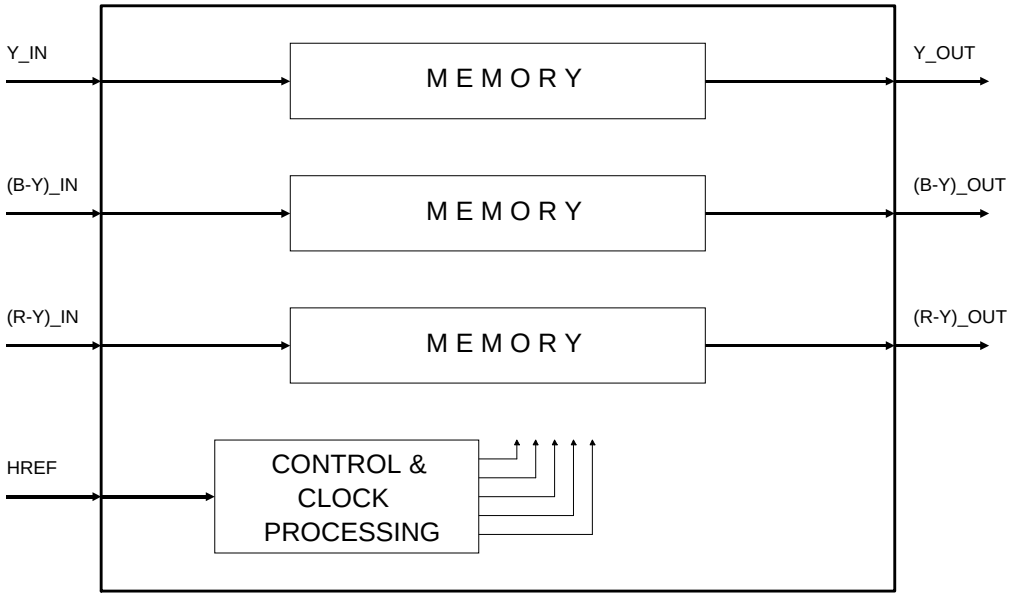


Fig. 3: Functional Blockdiagram of a 16:9 Compressor

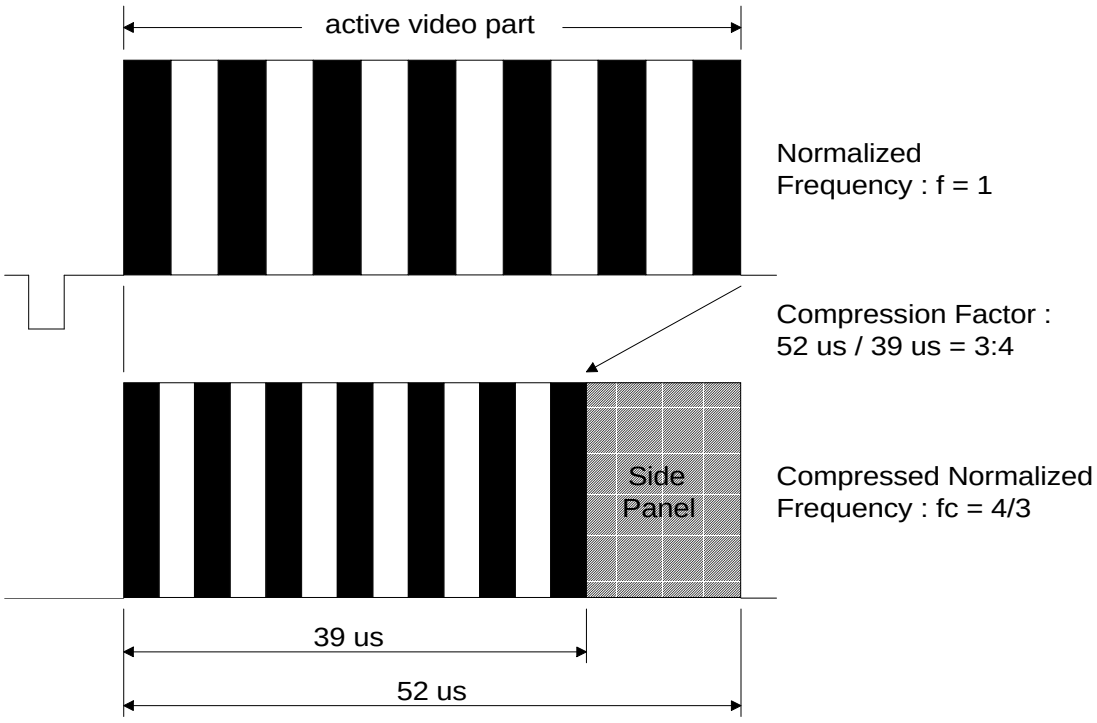


Fig. 4: Time Compression and Frequency Shifting

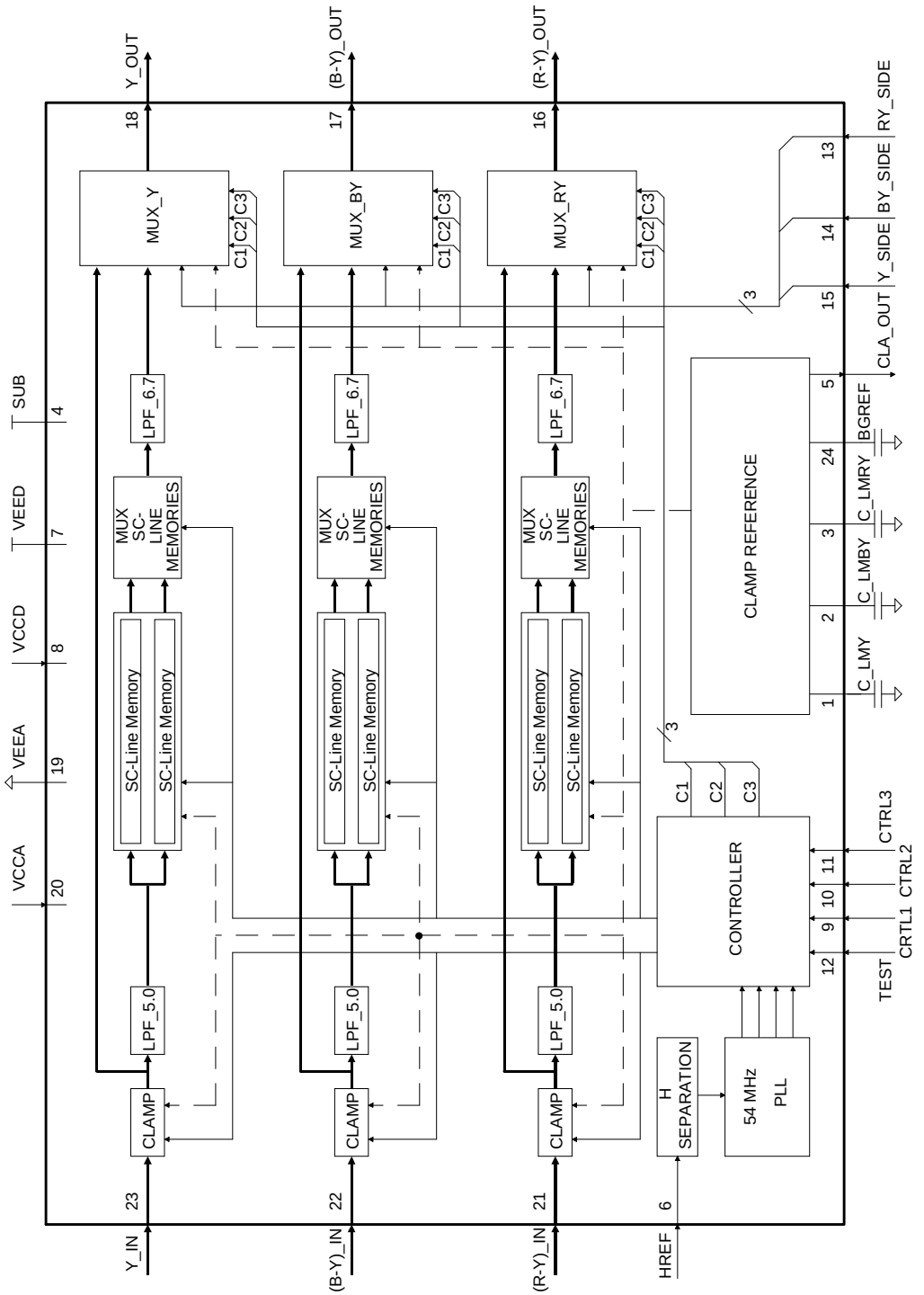


Fig. 5: Blockdiagram of the 16:9 Compressor SAA4981

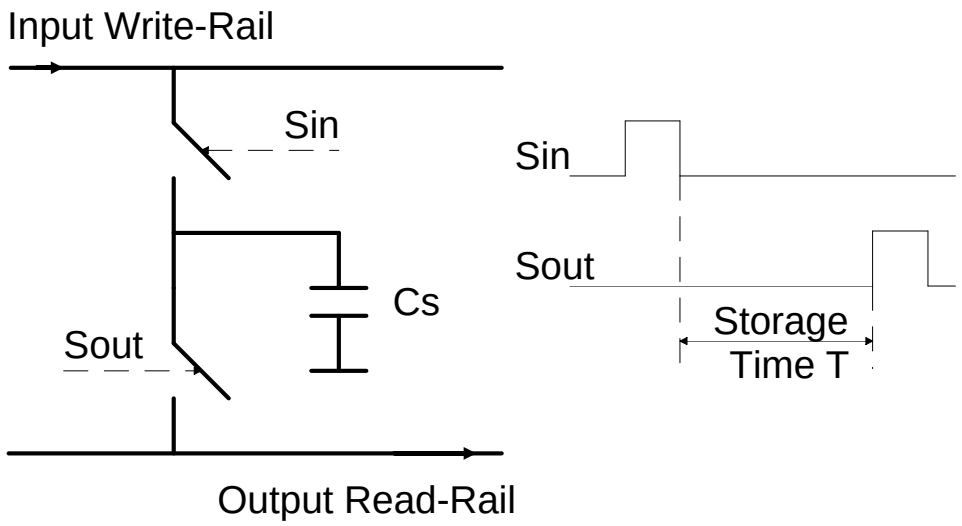


Fig. 6: Switched-Capacitor Memory Cell

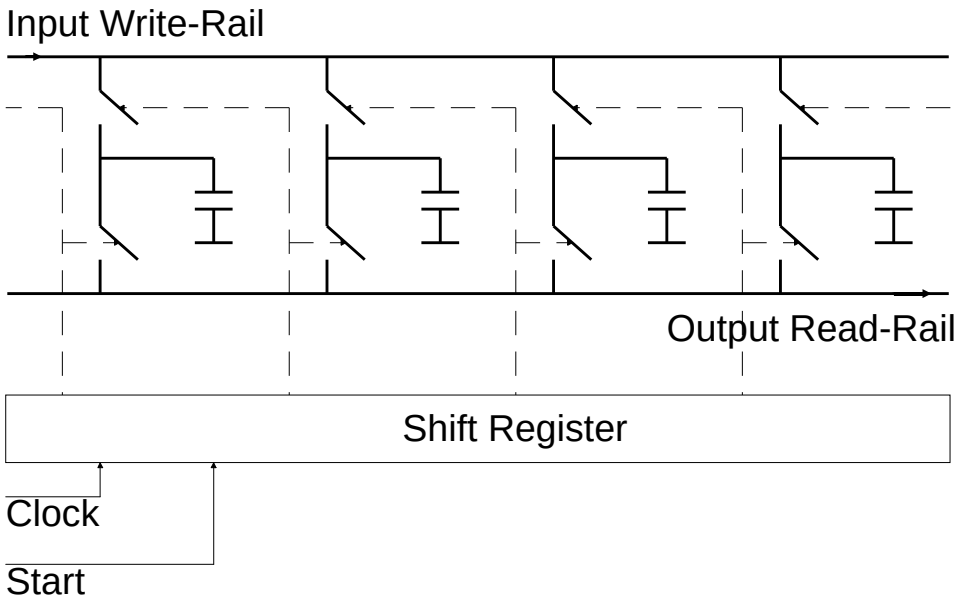


Fig. 7: Switched-Capacitor Line Memory

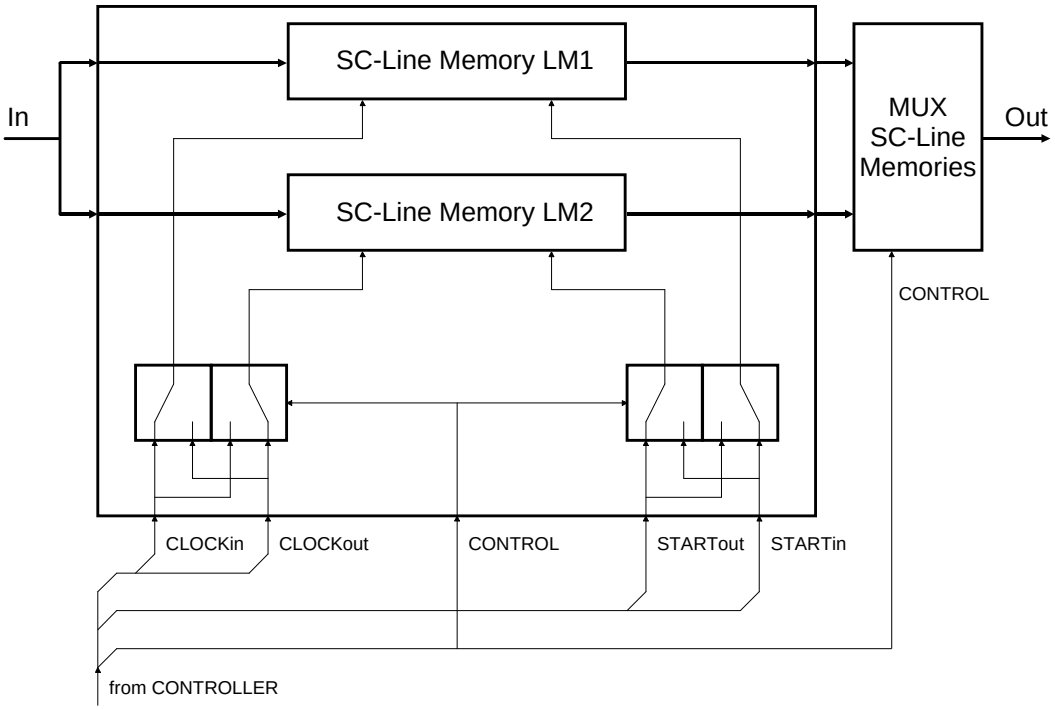


Fig. 8: Line Memory Configuration of the 16:9 Compressor

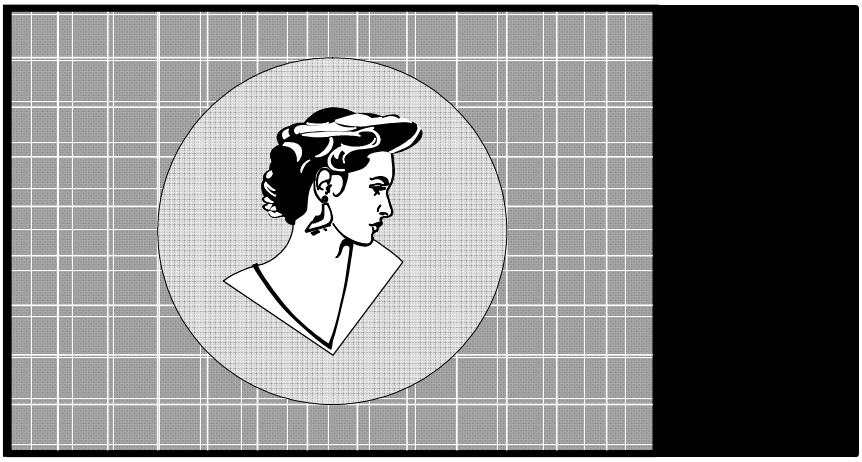


Fig. 9.1: Compression Mode, Left Position

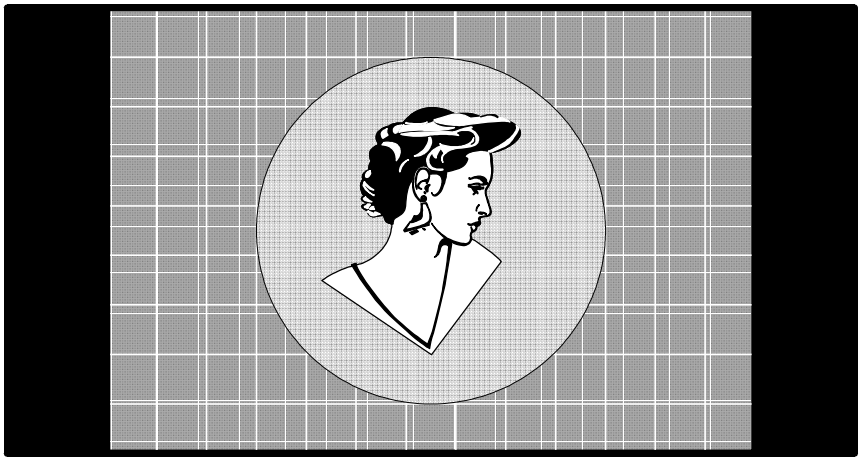


Fig. 9.2: Compression Mode, Centre Position

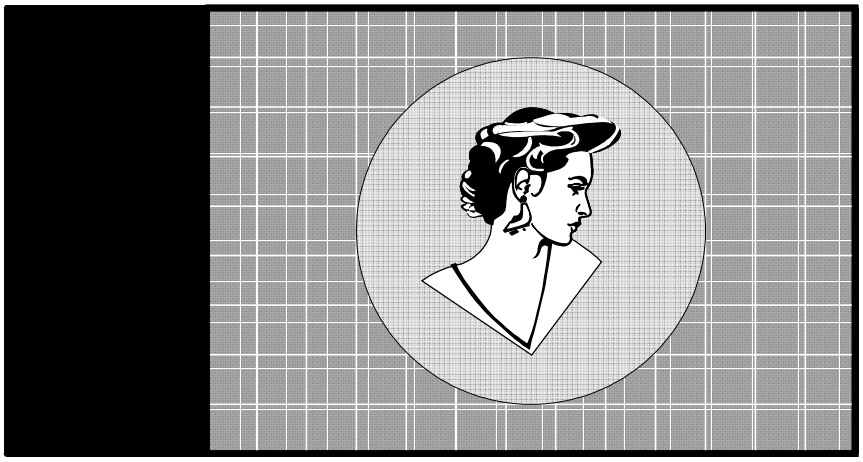
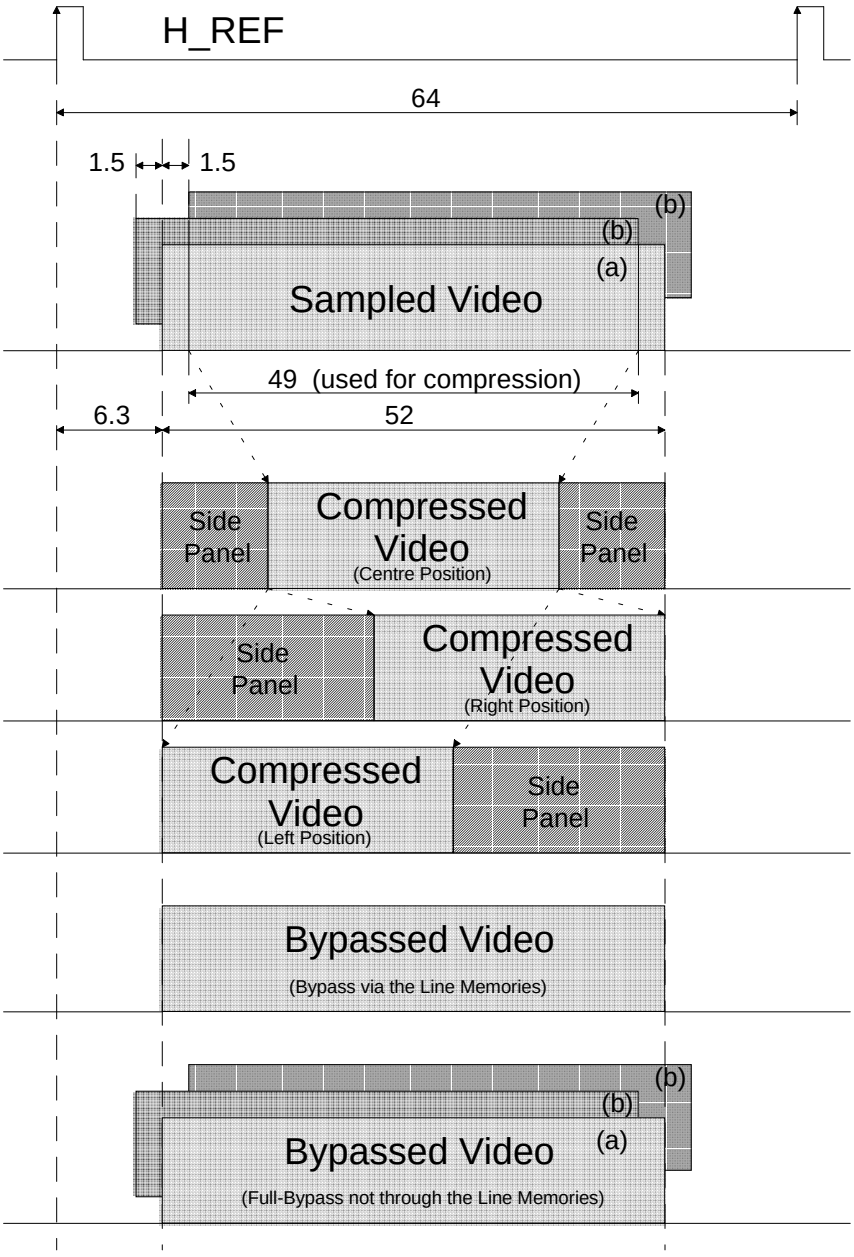


Fig. 9.3: Compression Mode, Right Position



Rem.: (a) Nominal timing for a 52us active video signal to generate a centred compressed video signal
(b) Worst-case picture position for a 52us active video signal to generate no visible blanking between side panels and compressed video
(c) All times in us.

Fig. 10: Horizontal Timing

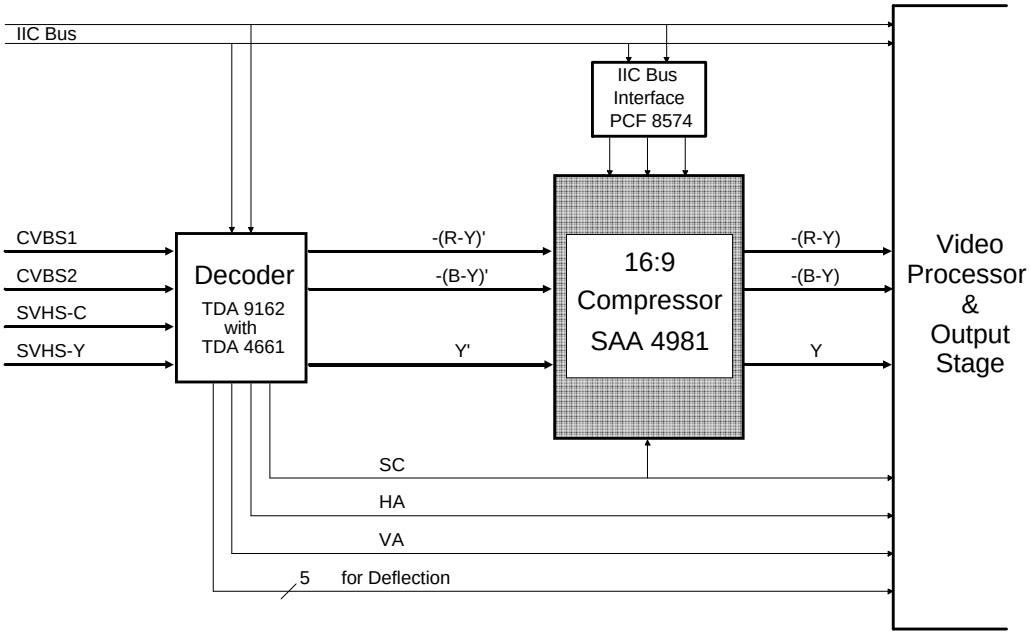


Fig. 11: System Application Diagram with Colour Decoder TDA 9162/4661 and 16:9 Compressor SAA4981

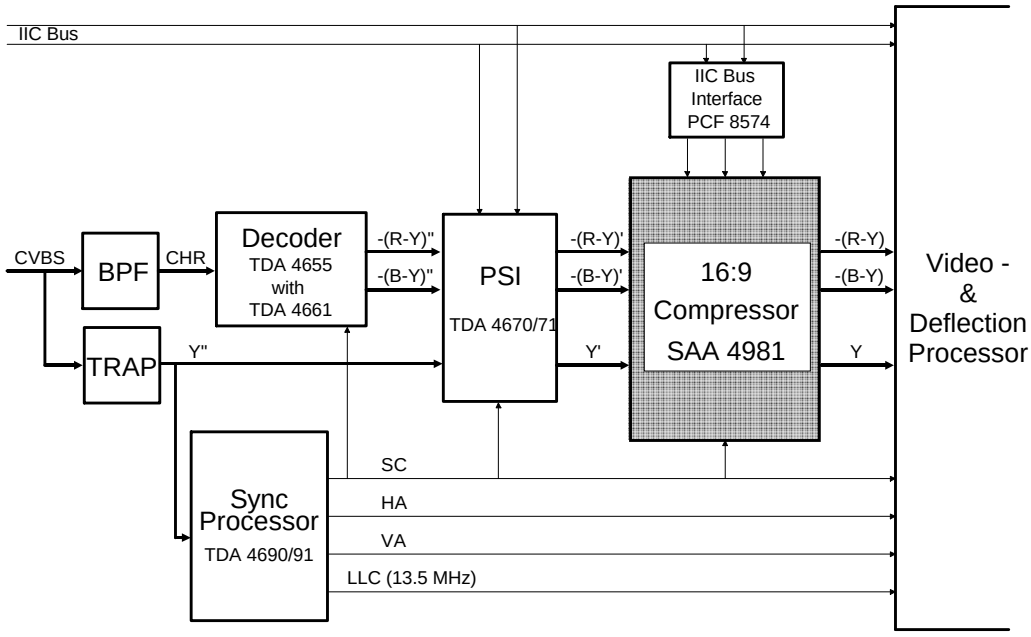


Fig. 12: System Application Diagram with Colour Decoder TDA4655/4661, Sync-Processor TDA4690/91, PSI TDA4670/71 and 16:9 Compressor SAA4981

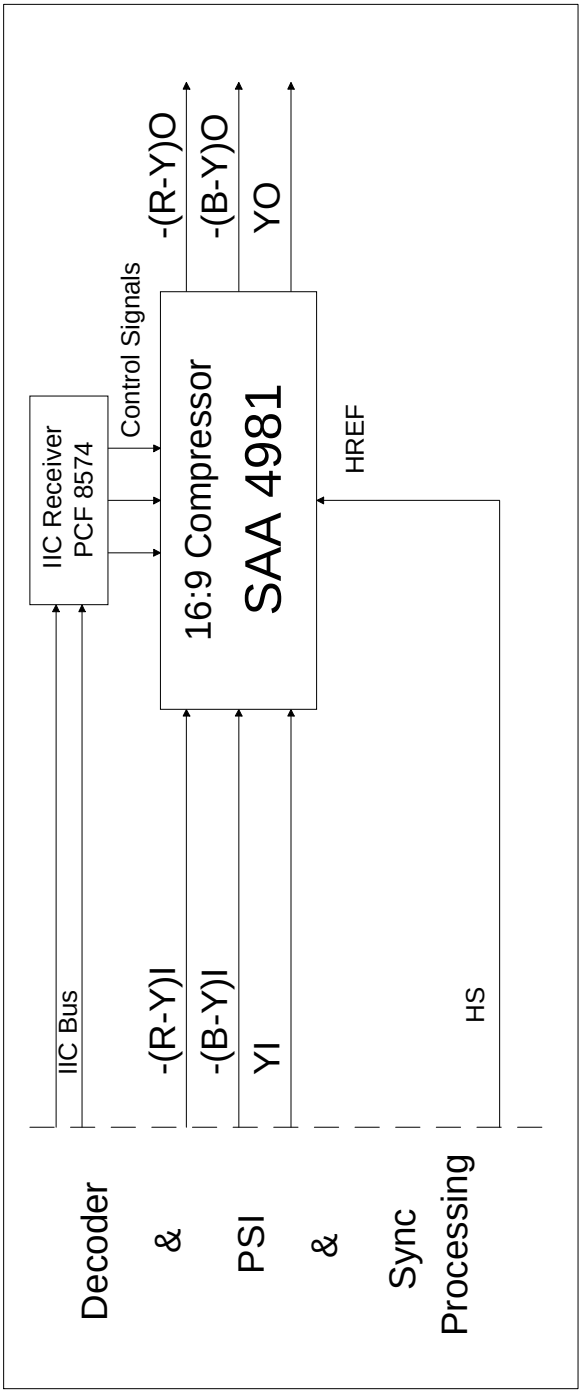


Fig. 13.1: Standard Application of the 16:9 Compressor SAA4981
Block diagram

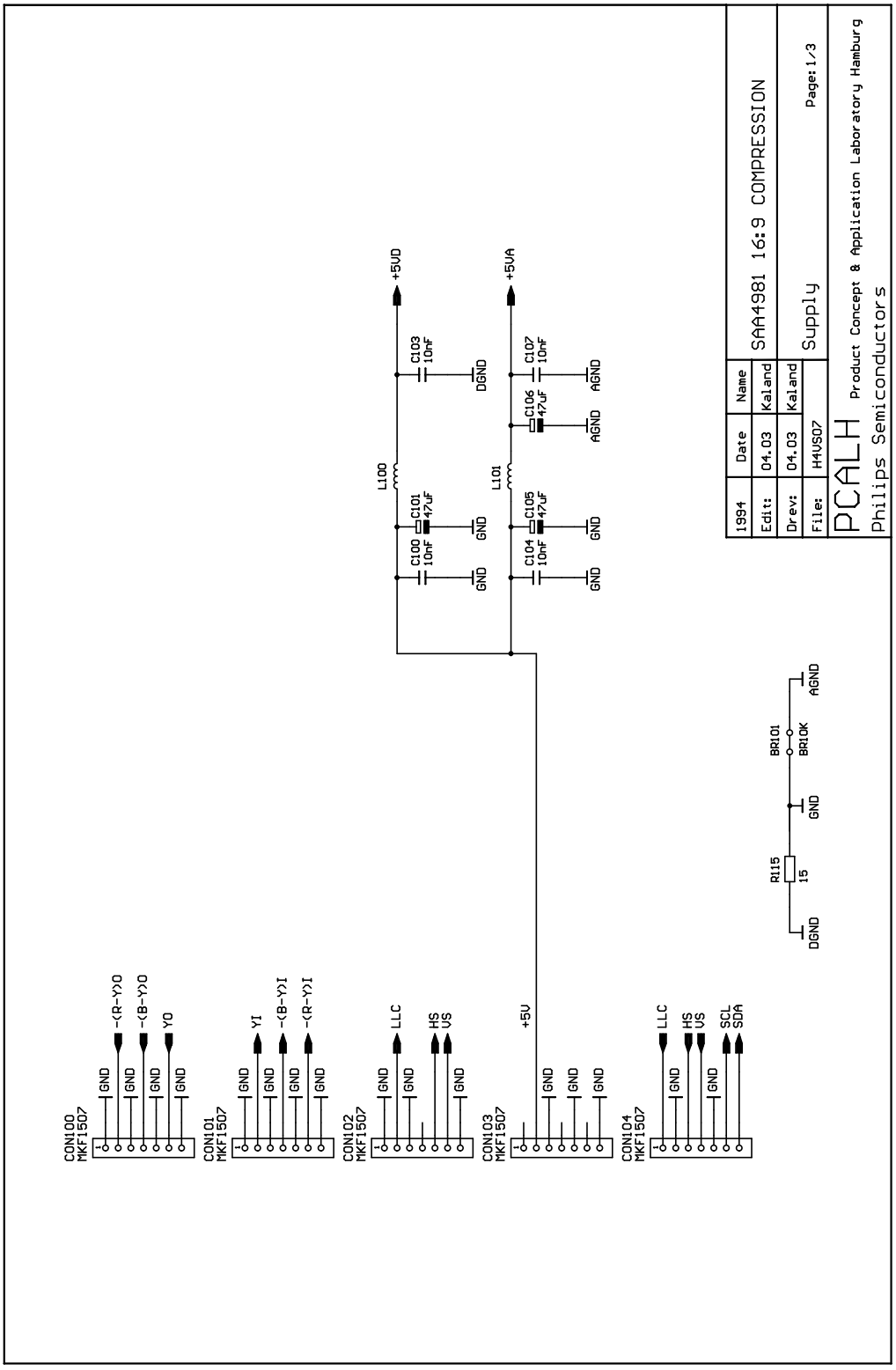


Fig. 13.2: Standard Application of the 16:9 Compressor SAA4981
Interface and Power supply

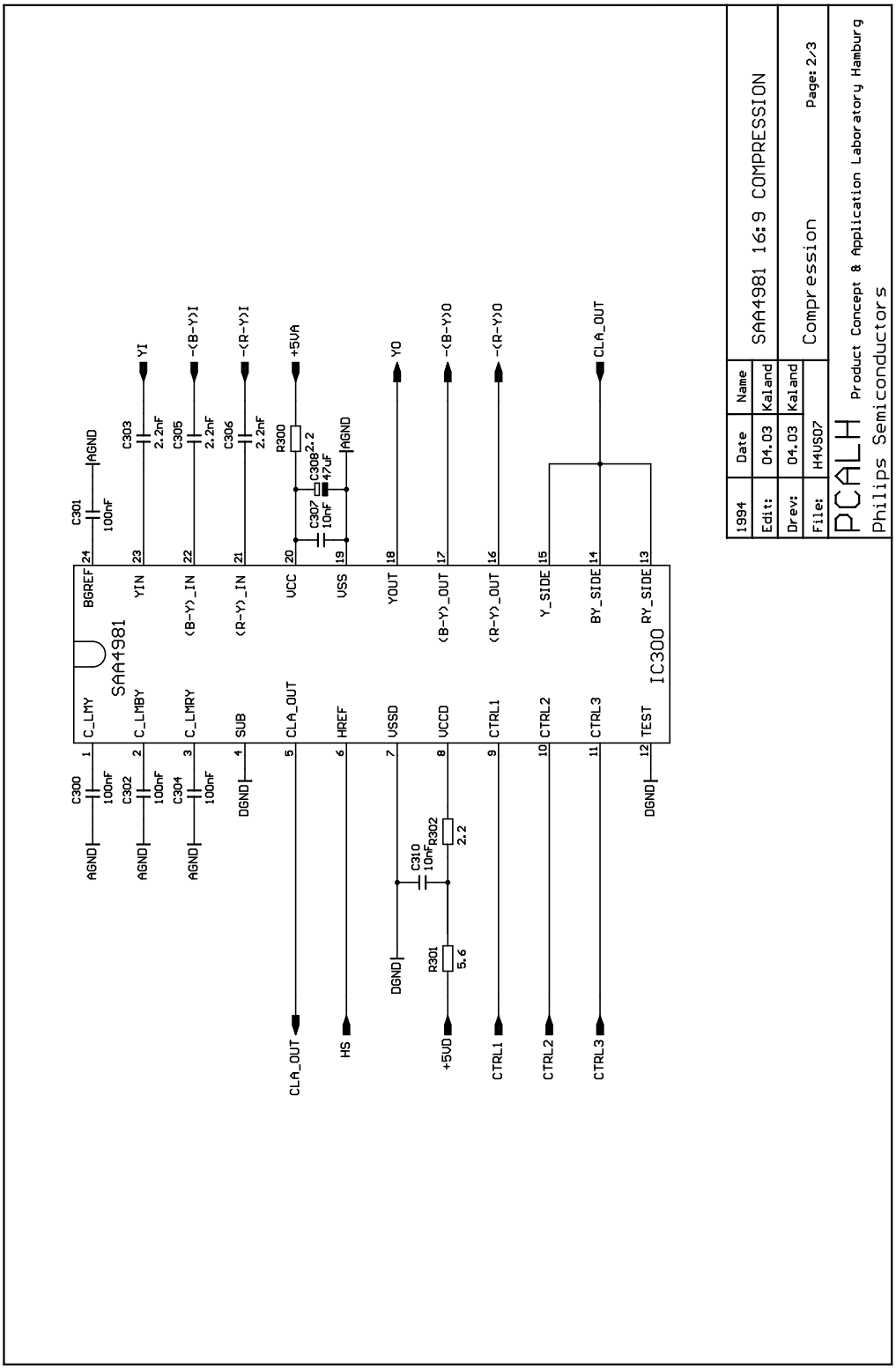


Fig. 13.3: Standard Application of the 16:9 Compressor SAA4981
SAA4981 application

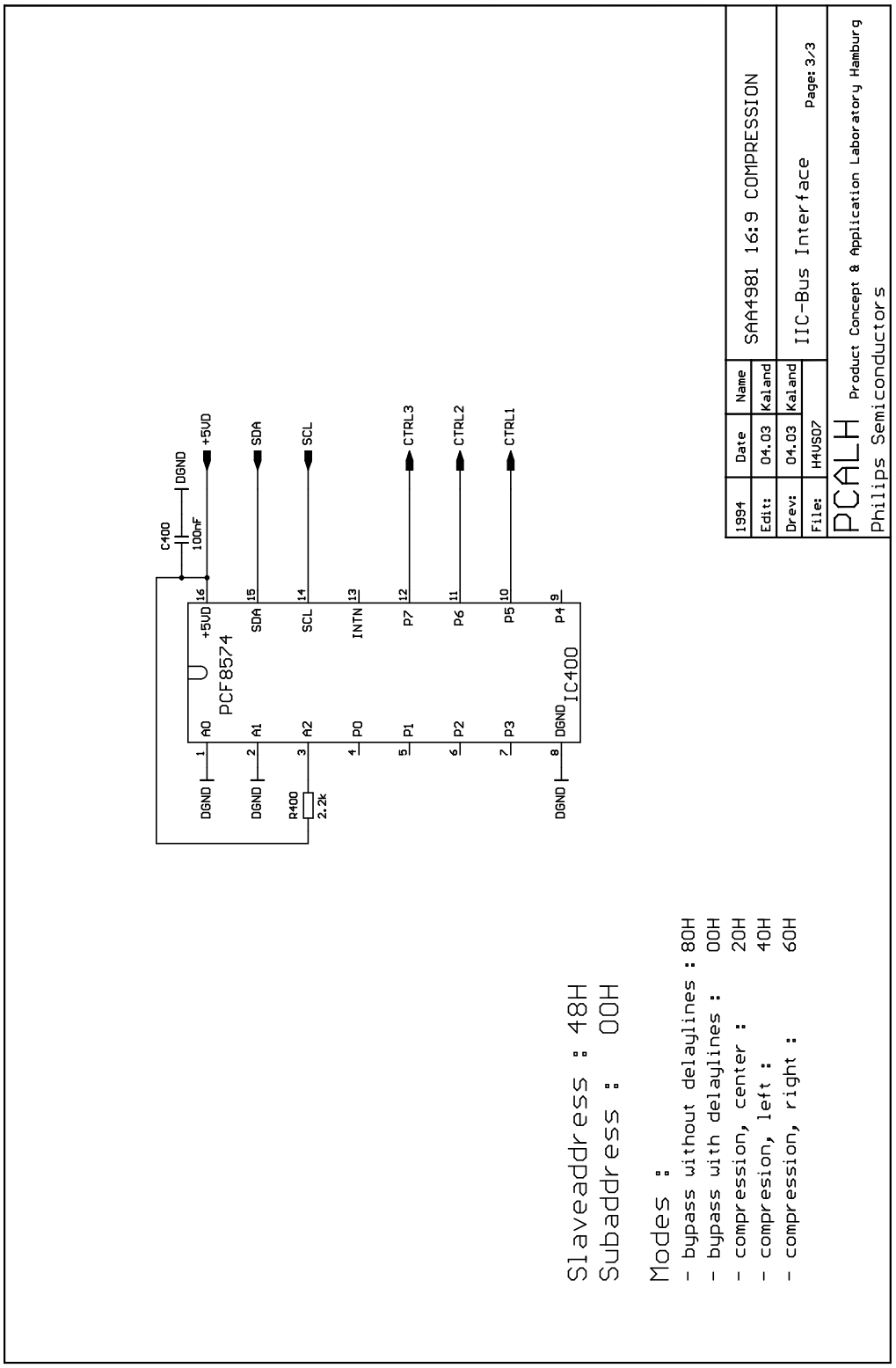


Fig. 13.4: Standard Application of the 16:9 Compressor SAA498
Control signal Generation with PCF8574

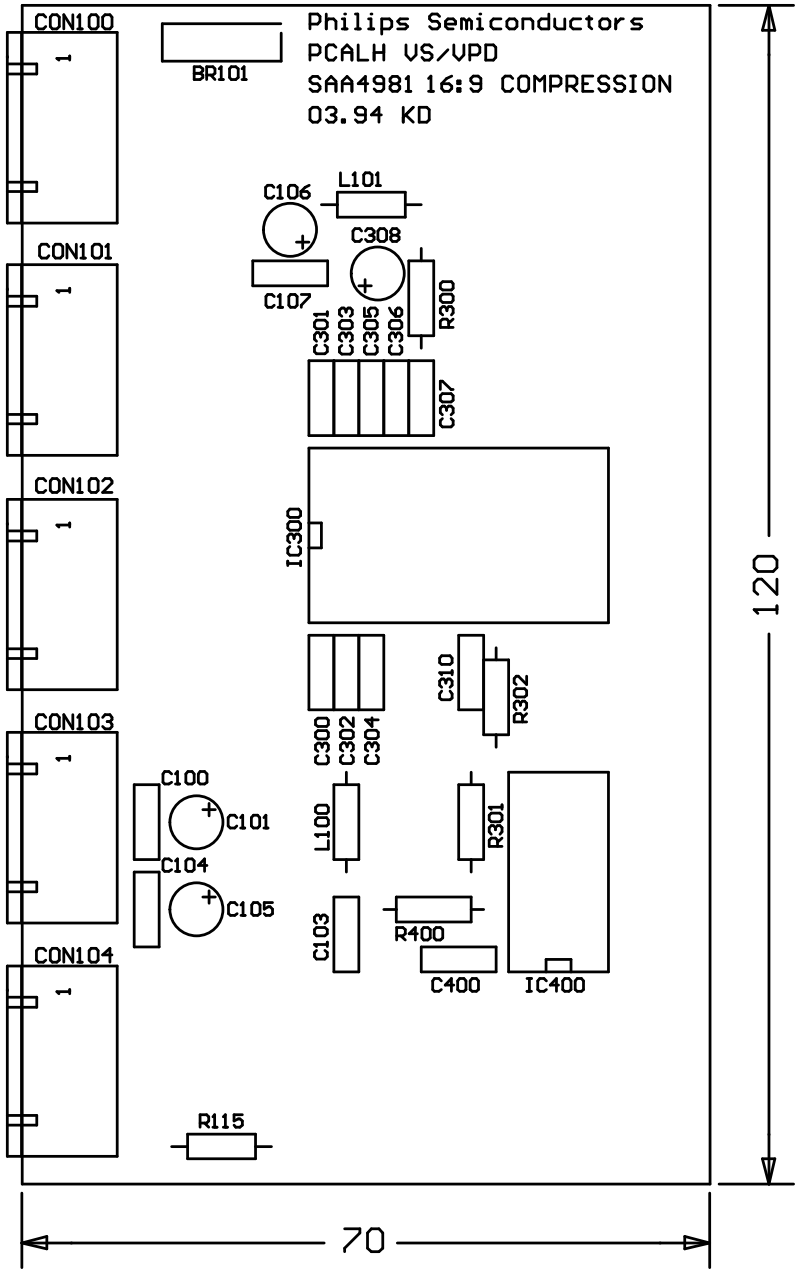


Fig. 13.5: Standard Application of the 16:9 Compressor SAA4981
PCB Device Placement

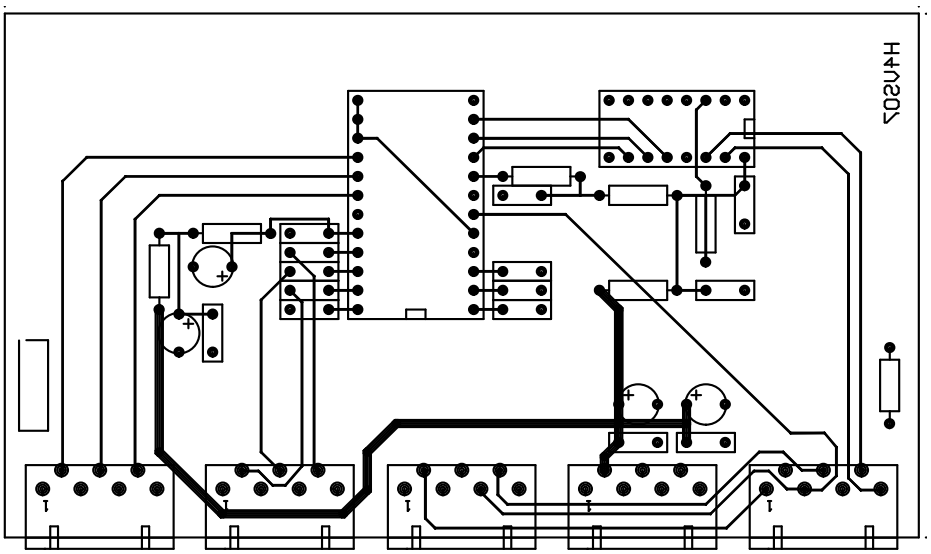


Fig. 13.6: Standard Application of the 16:9 Compressor SAA4981, PCB Bottom Layer

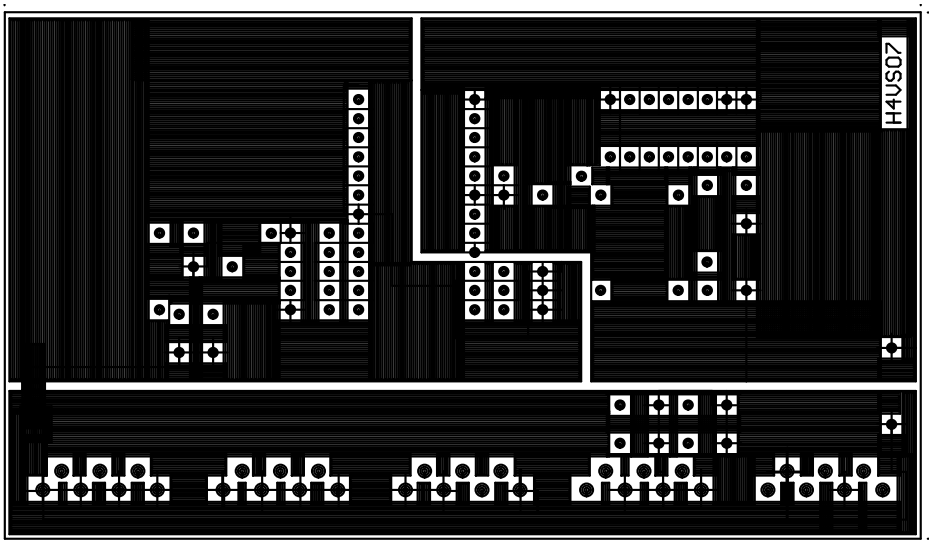


Fig. 13.7: Standard Application of the 16:9 Compressor SAA4981, PCB Top (Component) Layer

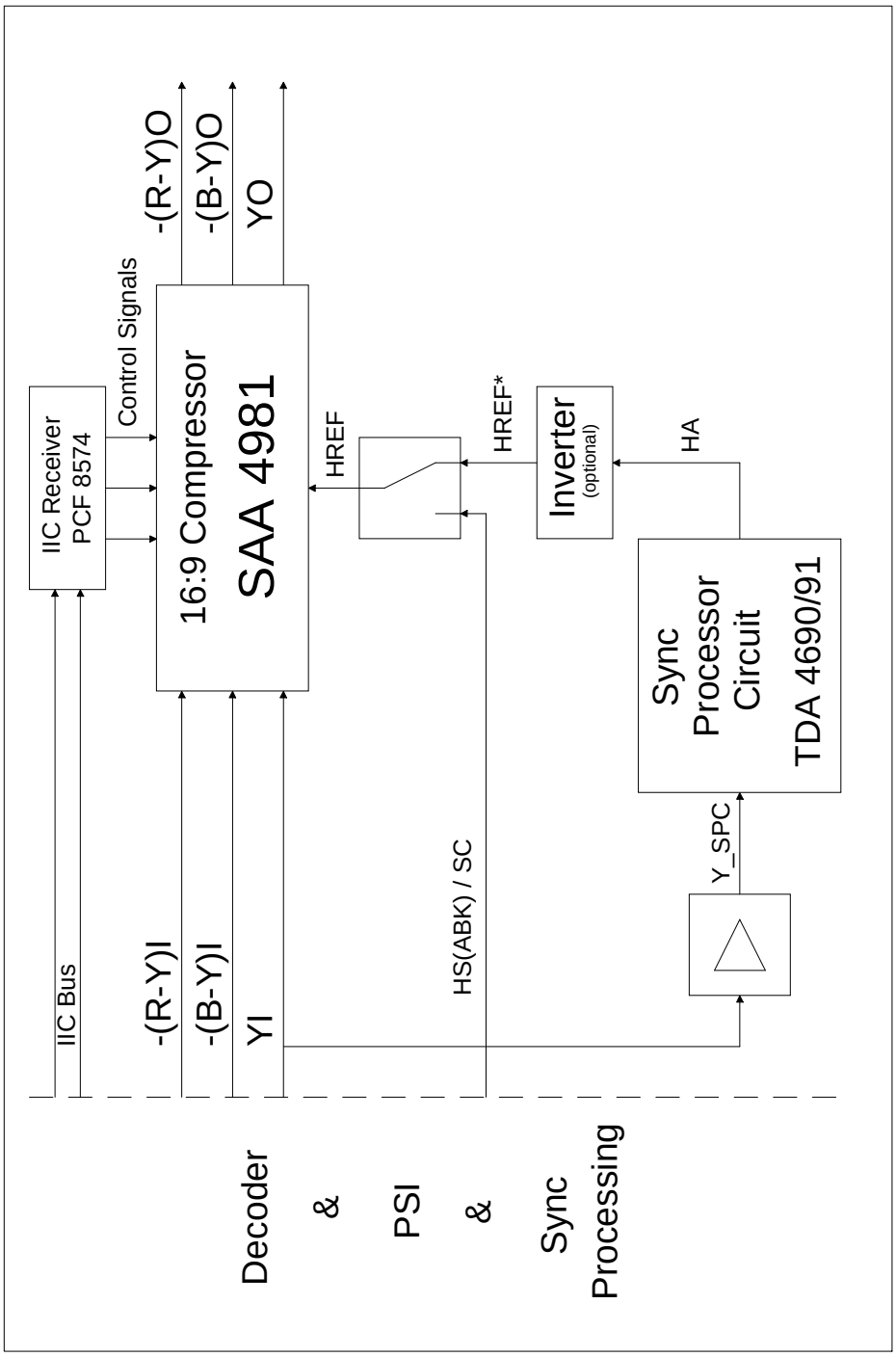


Fig. 14.1: Application of the 16:9 Compressor SAA4981 with Delay Compensated HREF Input Signal Block diagram

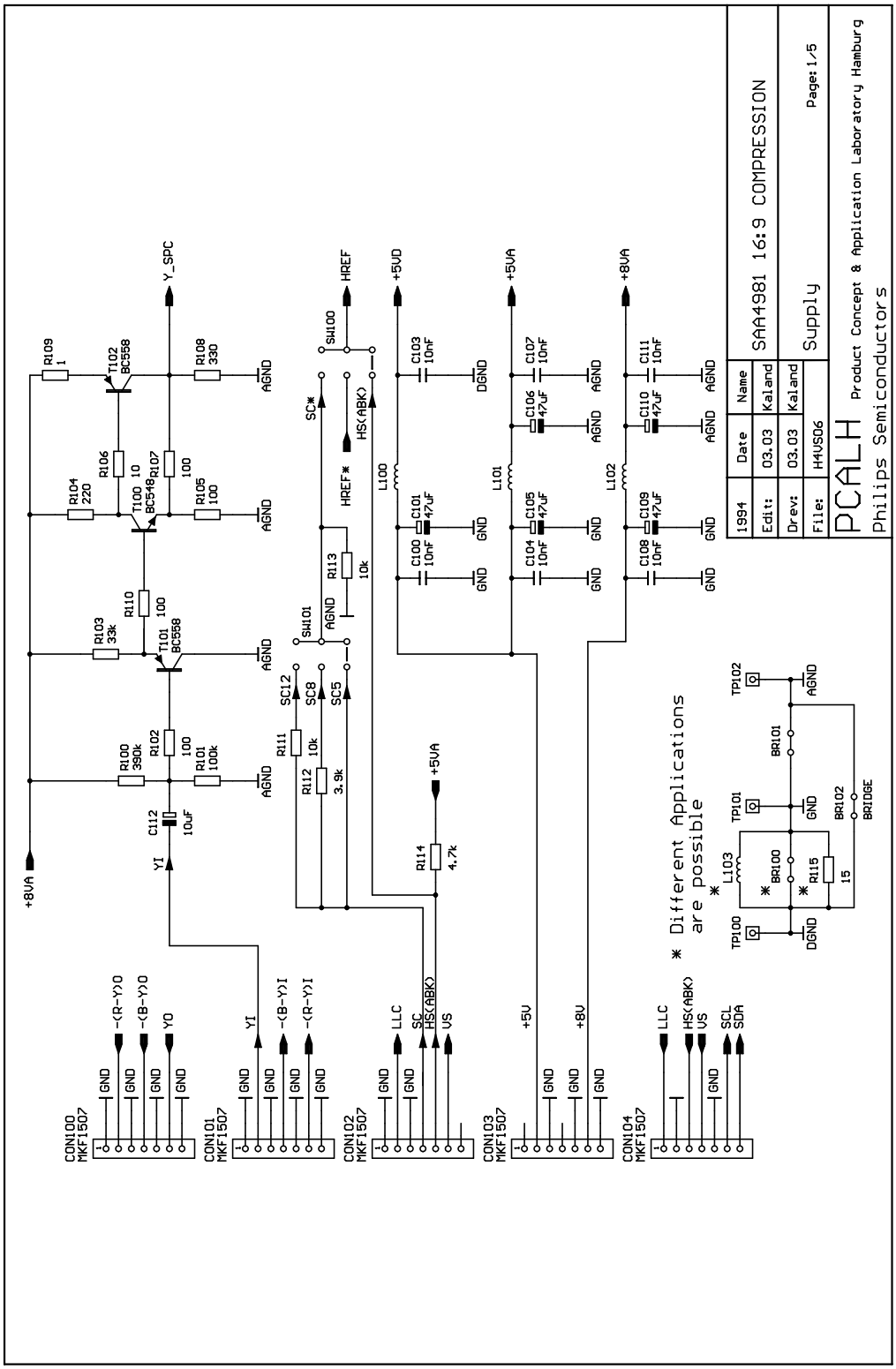


Fig. 14.2: Application of the 16:9 Compressor SAA4981 with Delay Compensated HREF Input Signal Interface and Power Supply

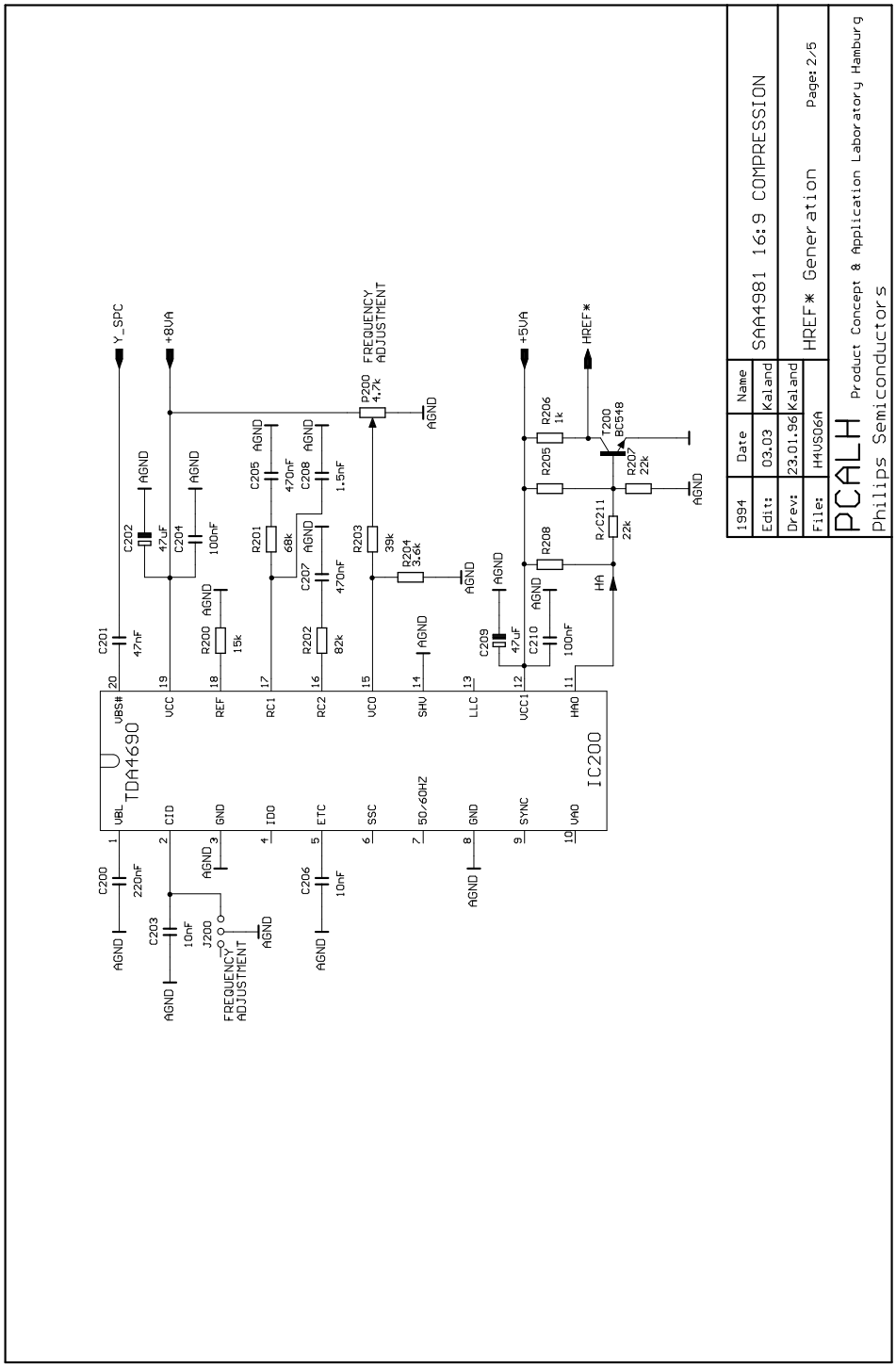


Fig. 14.3: Application of the 16:9 Compressor SAA4981 with Delay Compensated HREF Input Signal TDA4690 Application

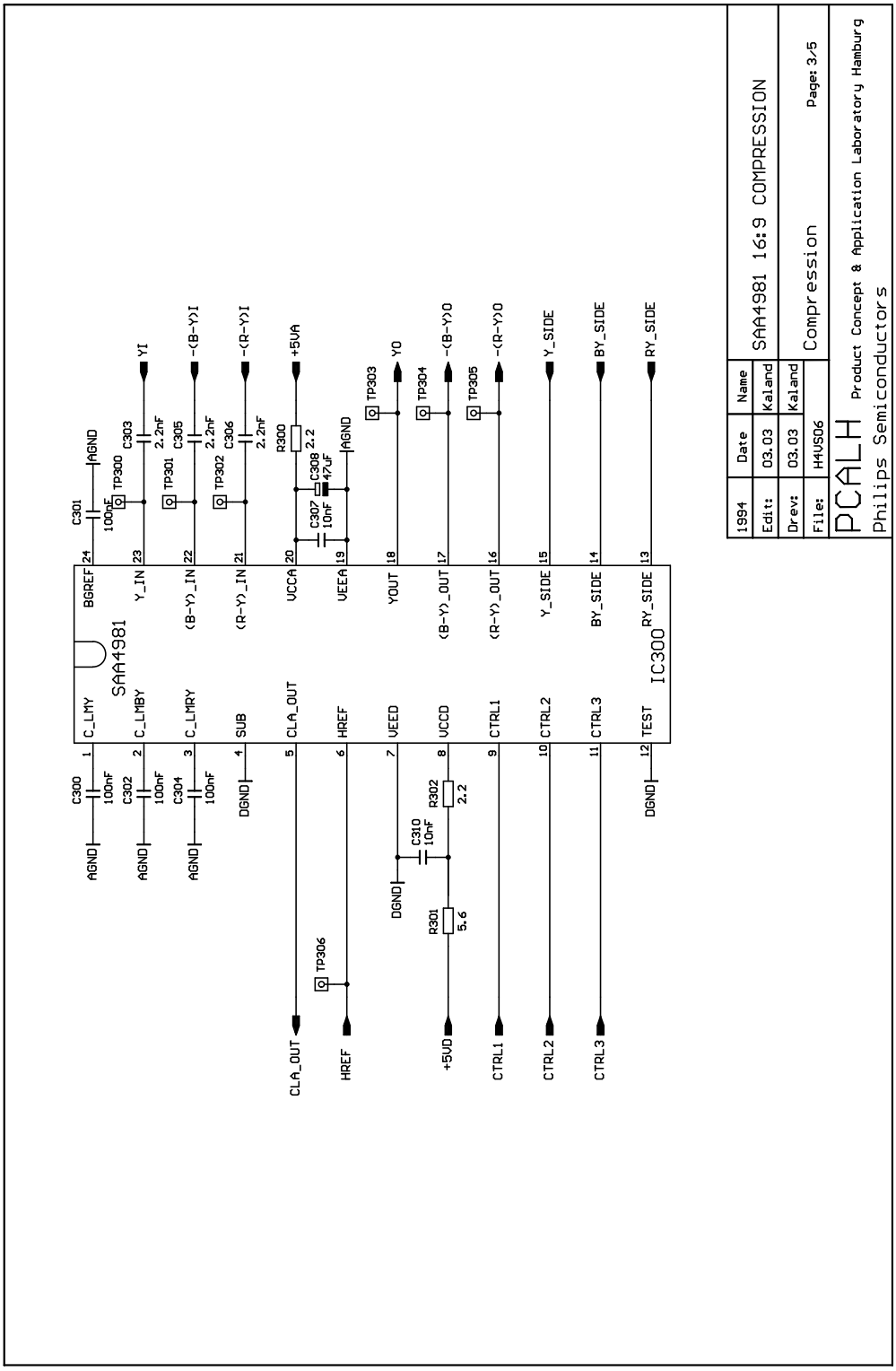


Fig. 14.4: Application of the 16:9 Compressor SAA4981 with Delay Compensated HREF Input Signal
SAA4981 Application

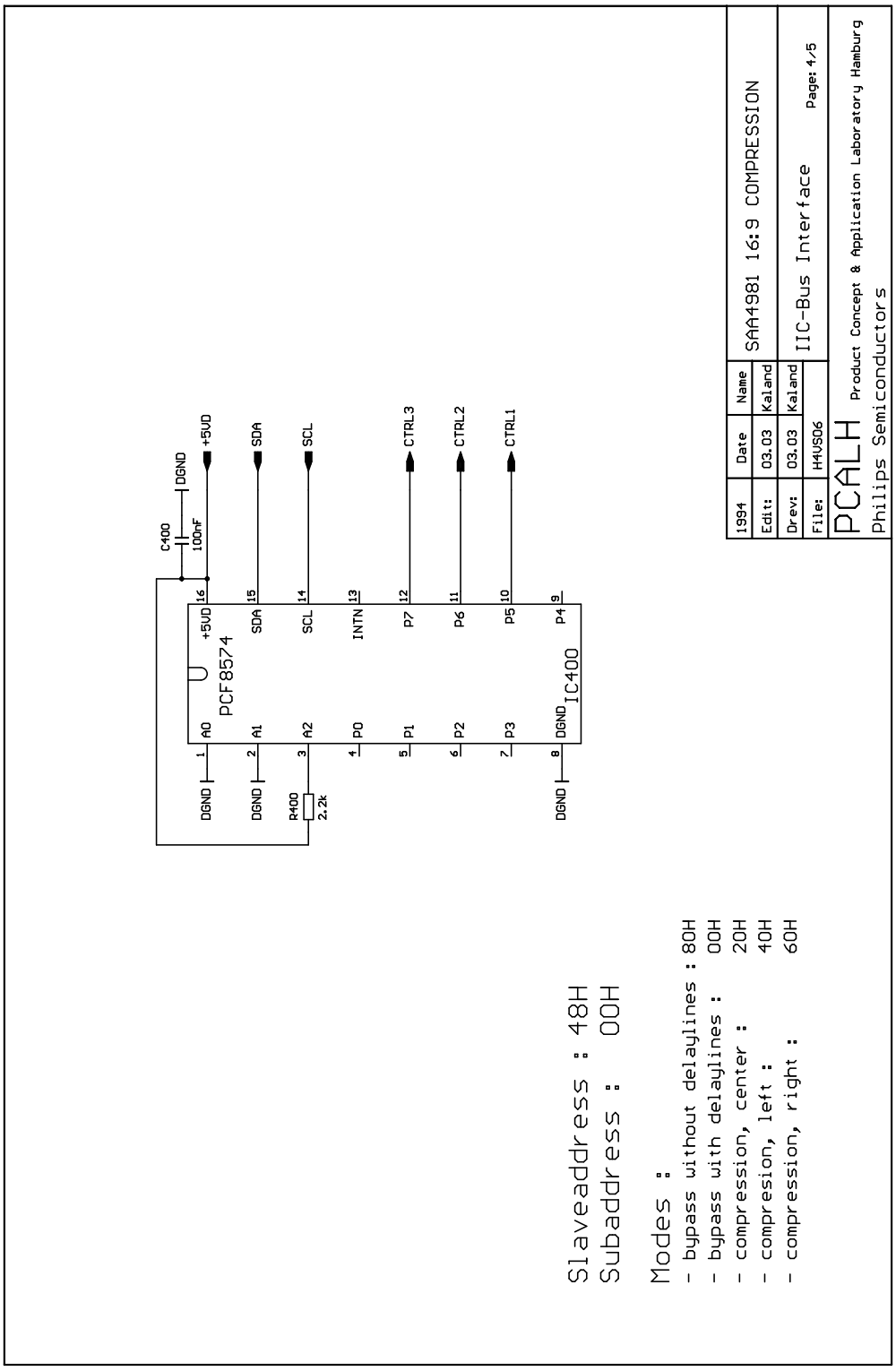


Fig. 14.5: Application of the 16:9 Compressor SAA4981 with Delay Compensated HREF Input Signal Control Signal Generation with PCF8574

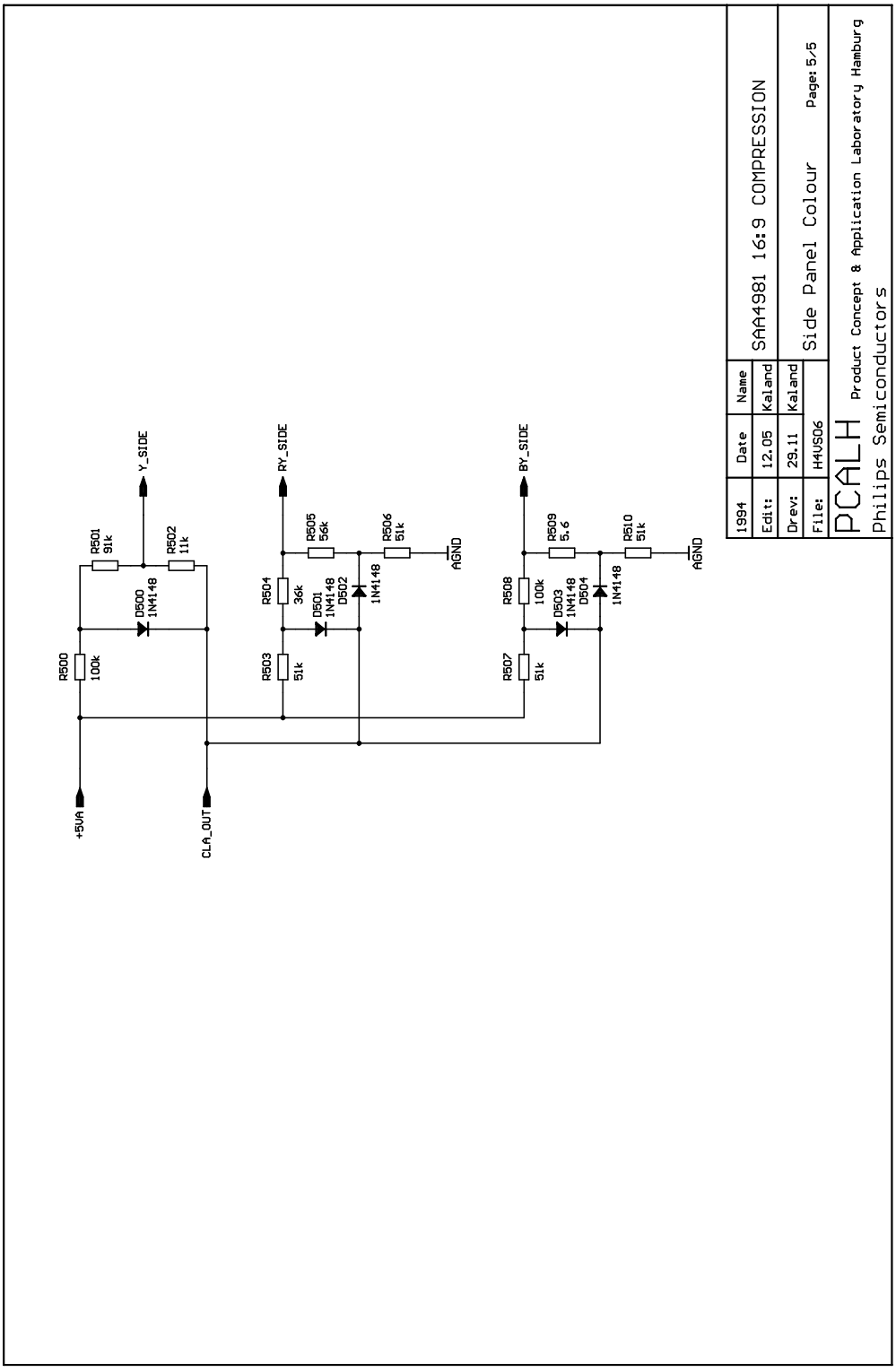


Fig. 14.6: Application of the 16:9 Compressor SAA4981 with Delay Compensated HREF Input Signal Side Panel Signal Generation

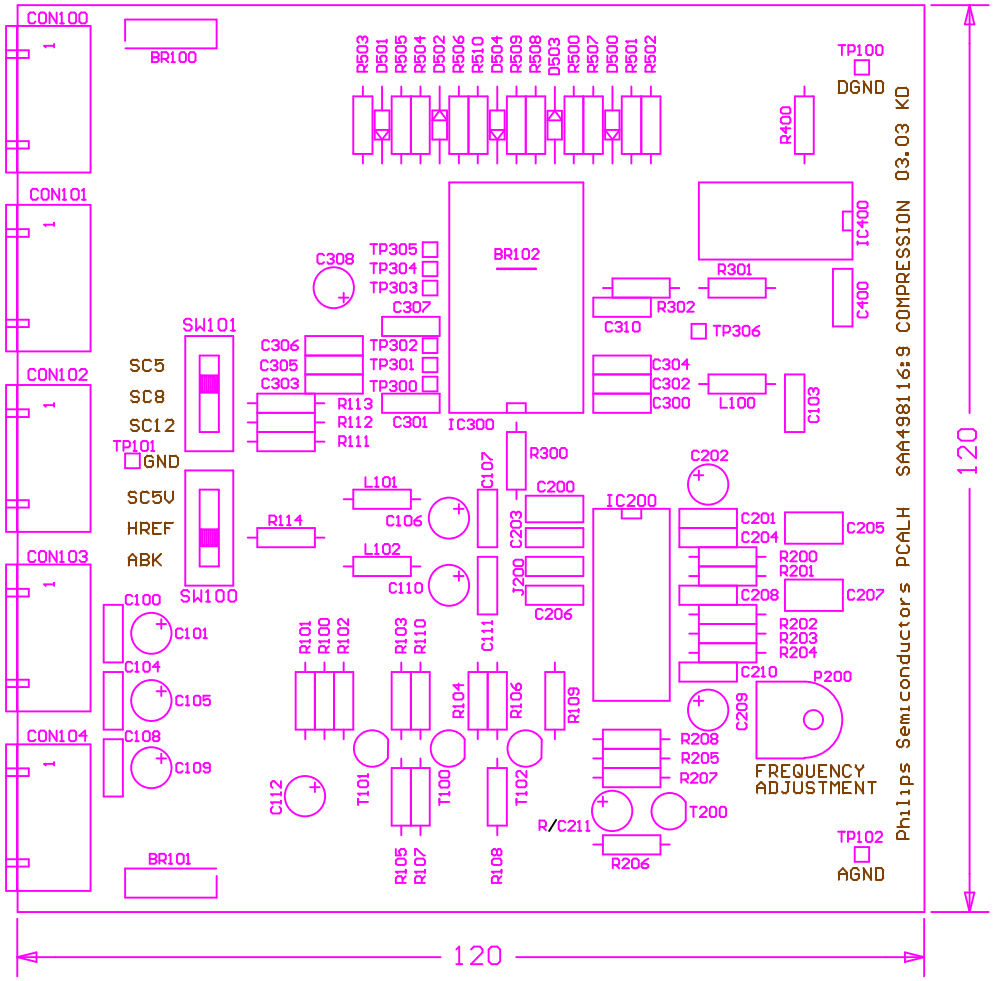


Fig. 14.7: Application of the 16:9 Compressor SAA4981 with Delay Compensated HREF Input Signal PCB Device Placement

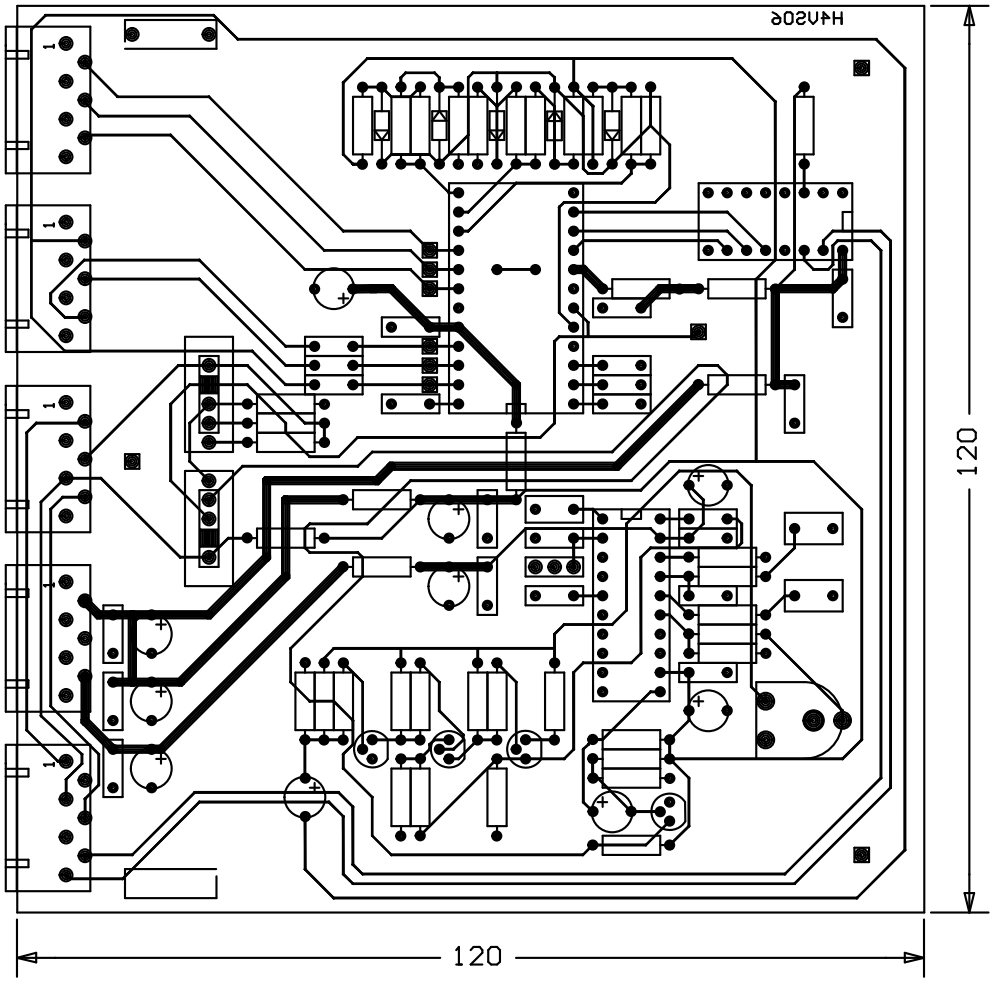


Fig. 14.8: Application of the 16:9 Compressor SAA4981 with Delay Compensated HREF Input Signal PCB Bottom Layer

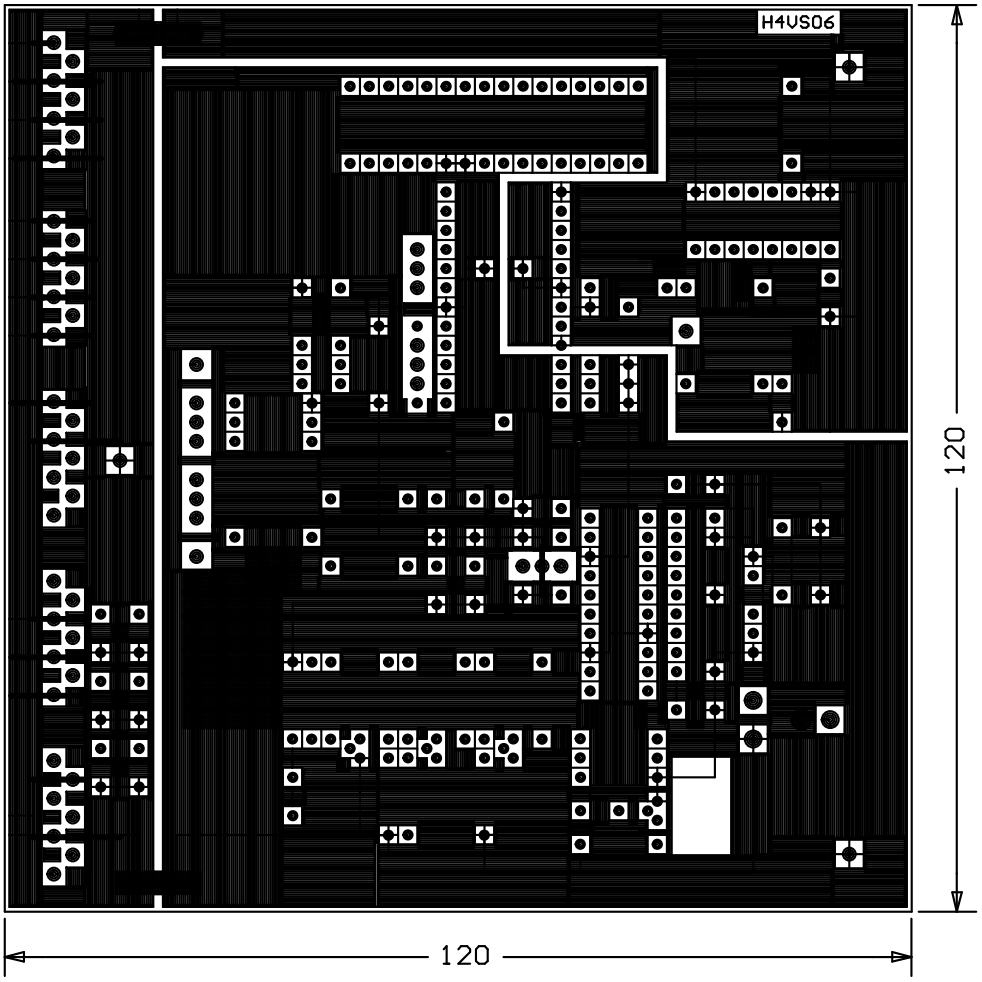
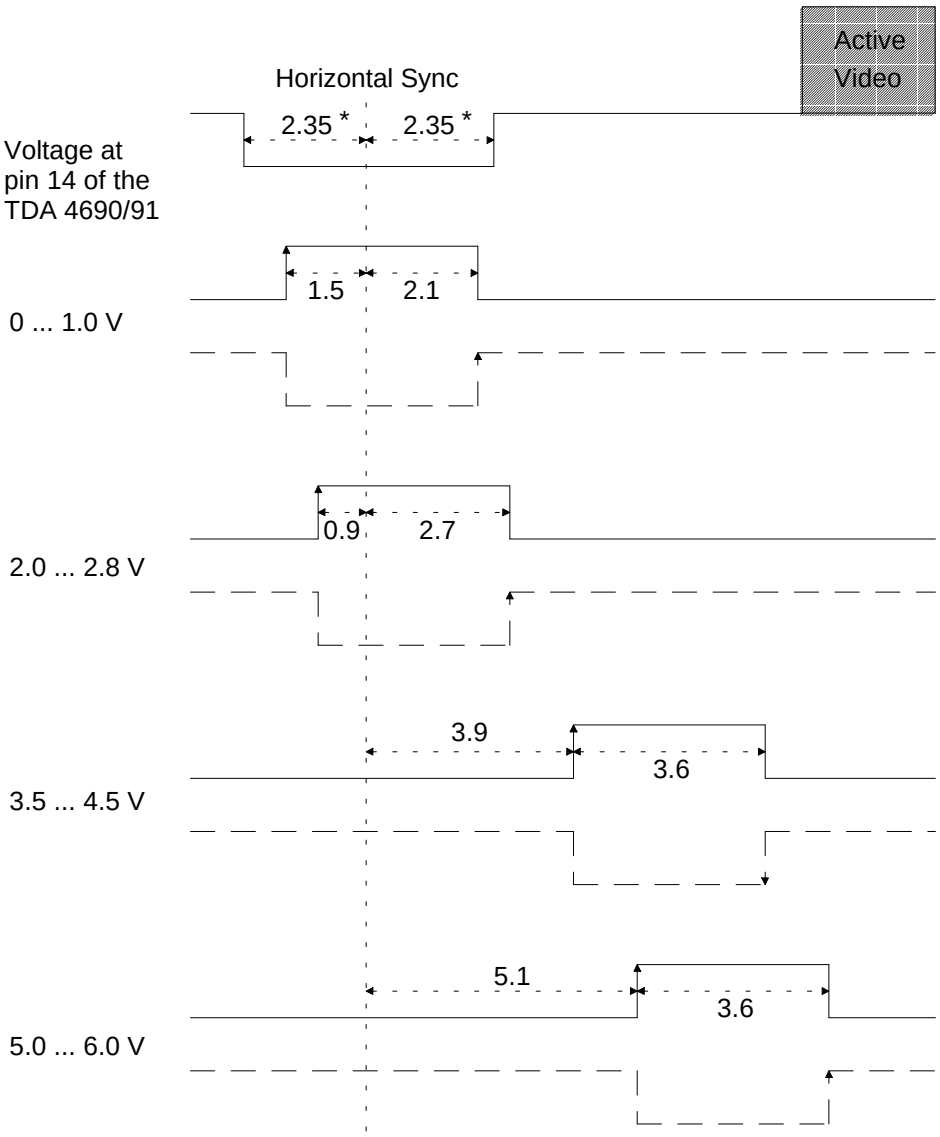


Fig. 14.9: Application of the 16:9 Compressor SAA4981 with Delay Compensated HREF Input Signal
PCB Top (Component) Layer



Remarks : ——— : H output of the TDA 4690/91

— – : Inverted H signal

All times in us

* sync timing for standards B, D, G, H, I, K, K1, L

Fig. 15: H Timing of the SPC TDA 4690/91

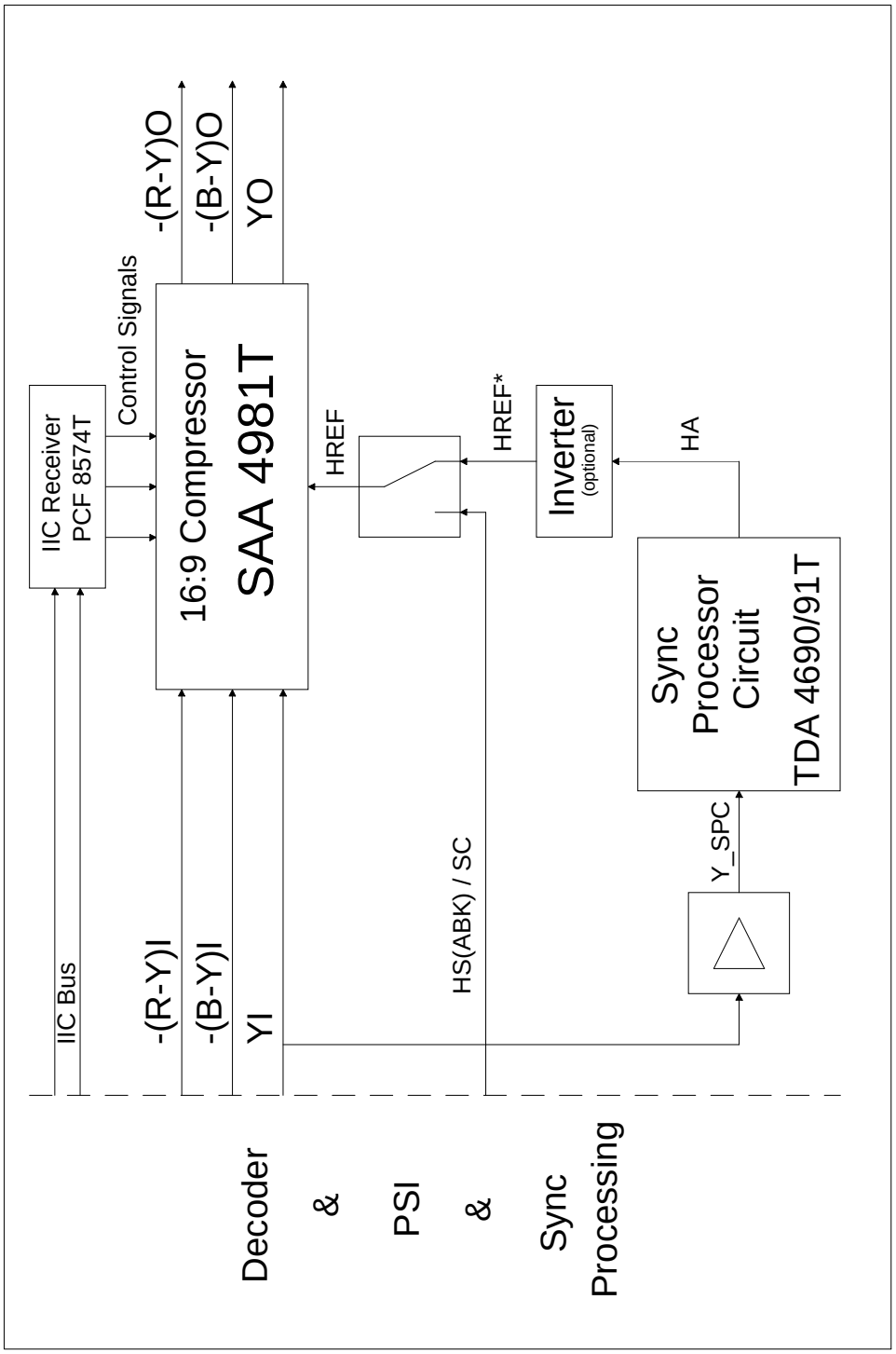


Fig. 16: Application of the 16:9 Compressor SAA4981T with Delay Compensated HREF Input Signal
Block diagram

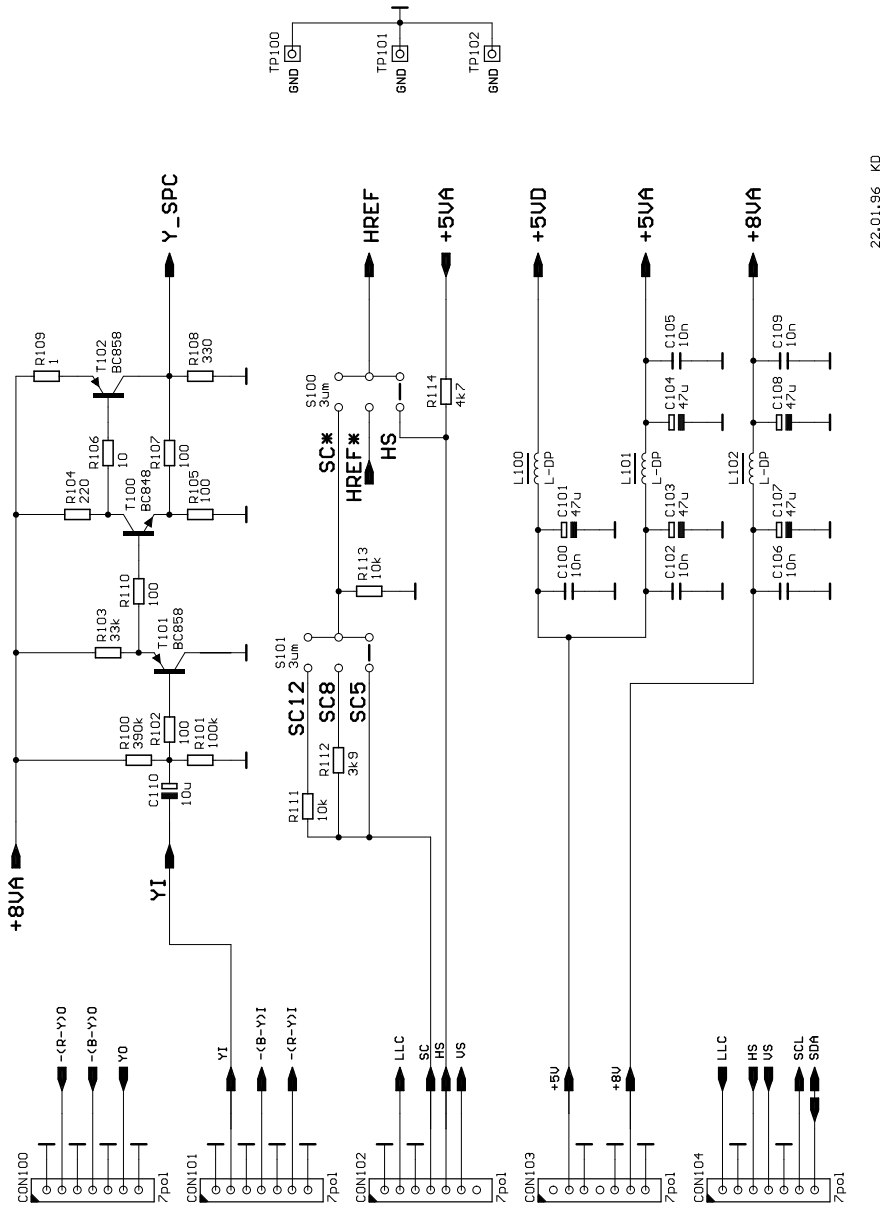


Fig. 16.1: Application of the 16:9 Compressor SAA4981TI Interface and Power Supply

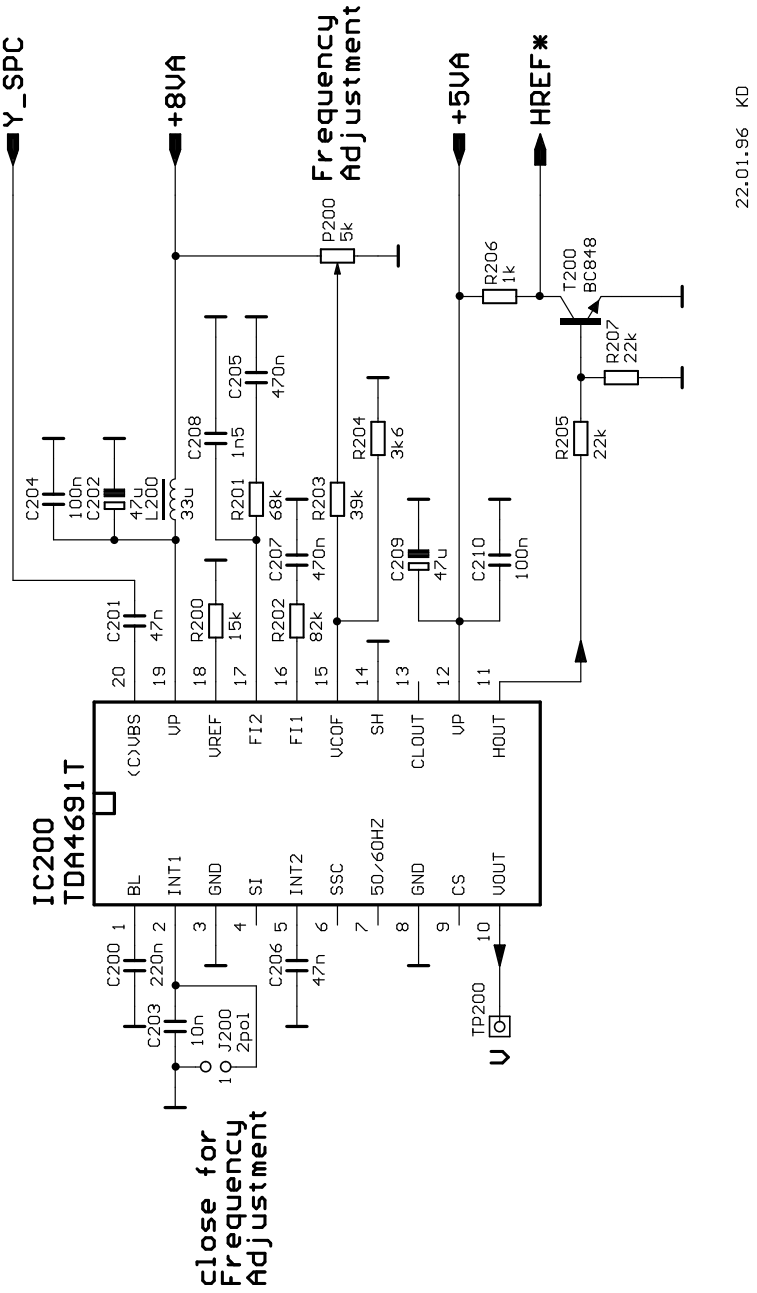


Fig. 16.2: Application of the 16:9 Compressor SAA4981T
TDA4691T Application

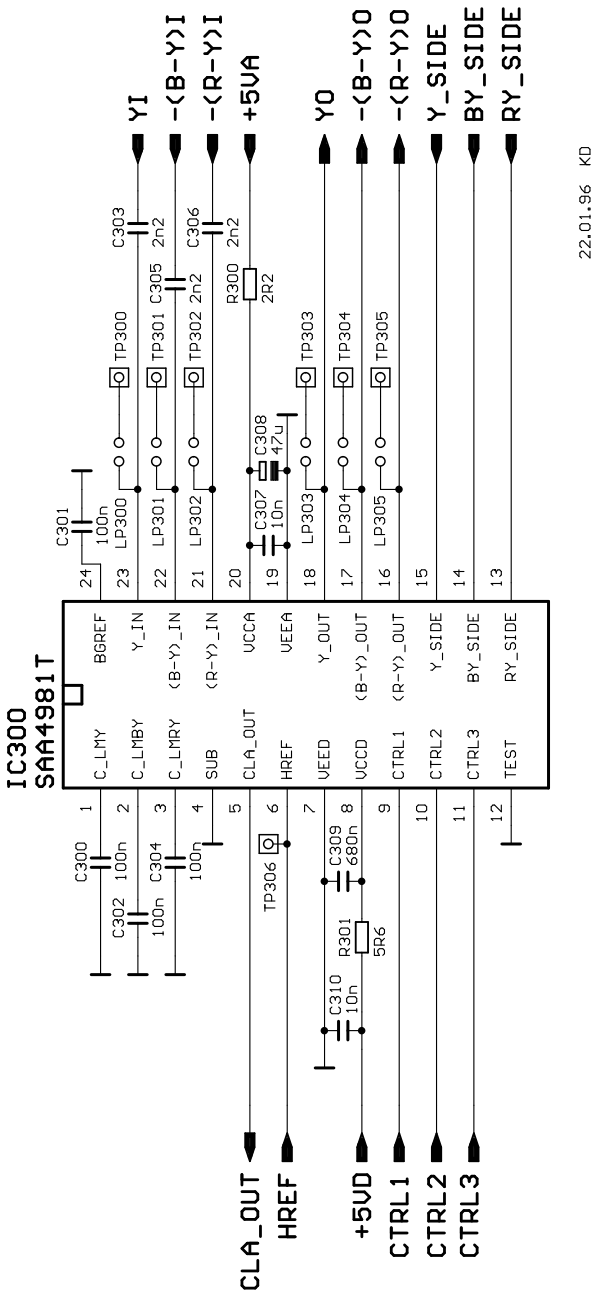
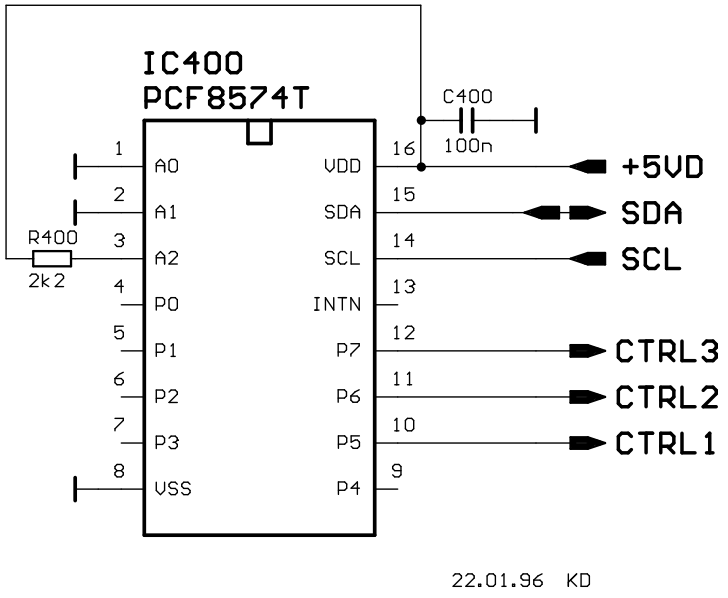


Fig. 16.3: Application of the 16:9 Compressor SAA4981T
SAA4981T Application



Slaveaddress: 48H
Subaddress: 00H

Modes:

- bypass not via line memories: 80H
- bypass via line memories: 00H
- compression, center: 20H
- compression, left: 40H
- compression, right: 60H

Fig. 16.4: Application of the 16:9 Compressor SAA4981T
Control Signal Generation with PCF8574T

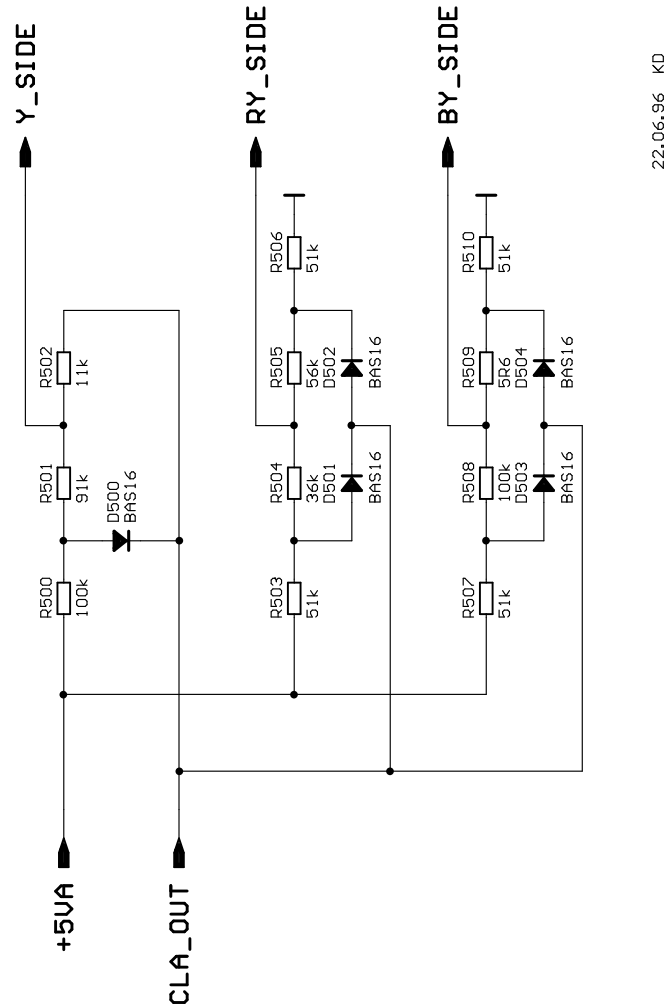


Fig. 16.5: Application of the 16:9 Compressor SAA498T
Side Panel Signal Generation

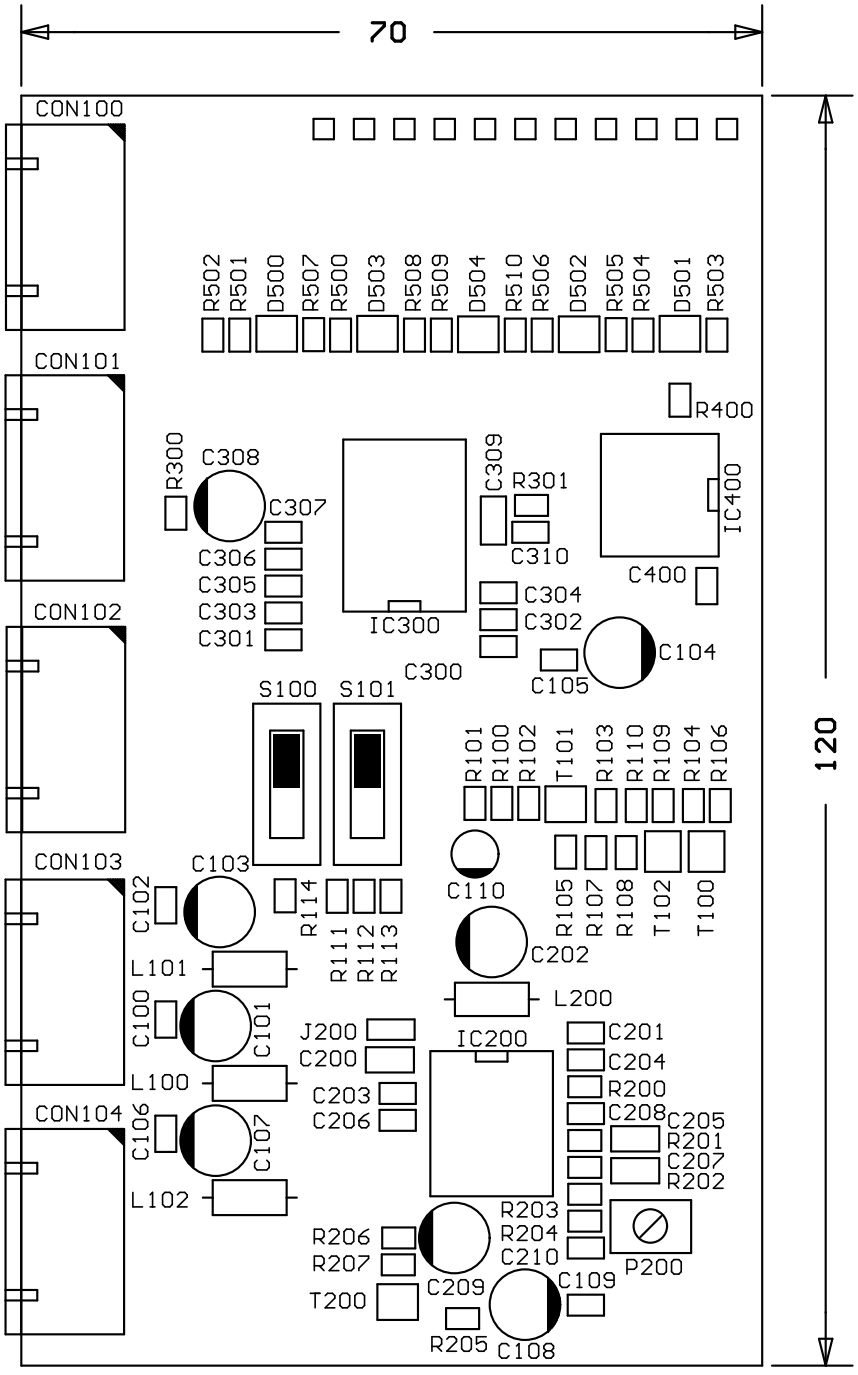


Fig. 16.6: Application of the 16:9 Compressor SAA4981T
PCB Device Placement

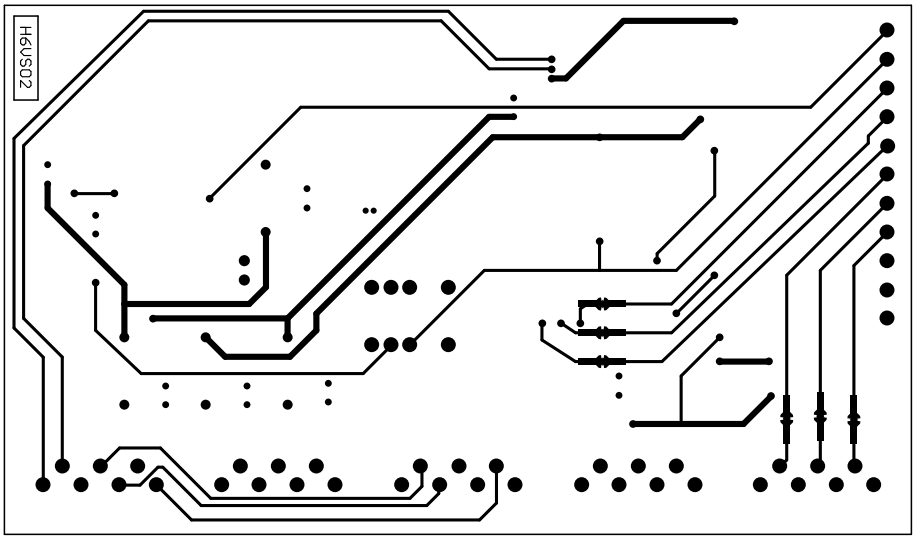


Fig. 16.7: Application of the 16:9 Compressor SAA4981T
PCB Bottom Layer

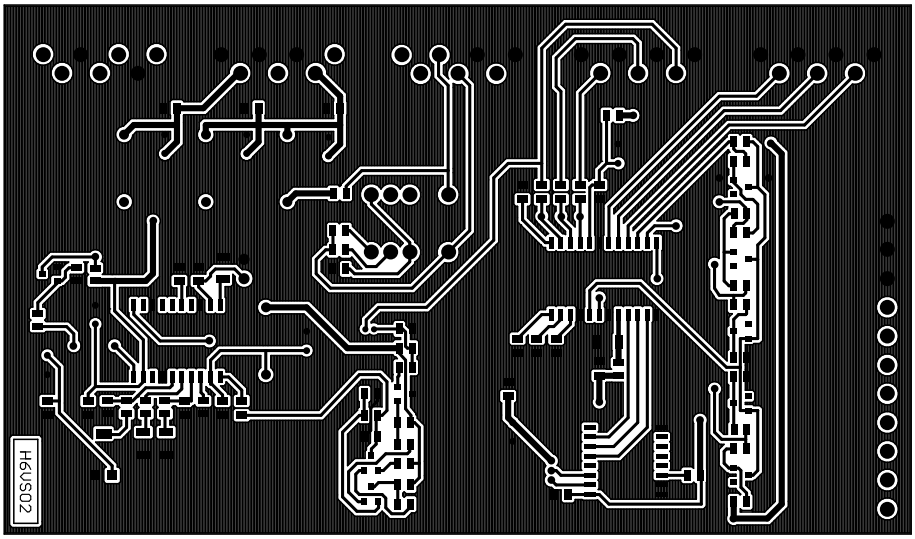


Fig. 16.8: Application of the 16:9 Compressor SAA4981Tl
PCB Top (Component) Layer